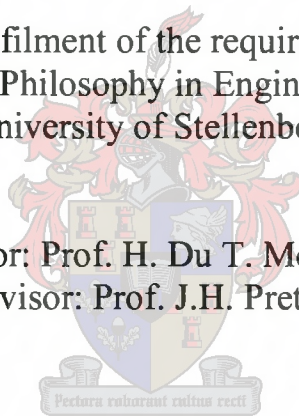

ANALYSIS AND SYNTHESIS OF AN INDUCTIVE STORAGE MILLISECOND PULSE FORMING NETWORK

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DECLARATION

I, the undersigned, hereby declare that the work contained in this dissertation is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted to any university for a degree.

SUMMARY

Millisecond pulse forming networks (PFNs) as applicable to electro-thermal chemical (ETC) loads fall into the <1 MJ energy bracket. The energy requirements of these loads require specialised power sources involving staged energy conversion. For the <1 MJ energy bracket, capacitive storage systems are usually employed. However, these systems exhibit low volume energy density and for volume sensitive applications; alternatives need to be considered.

Inductive storage supplies form a sub-group of the static supplies that have theoretically superior volume energy density characteristics.

This thesis documents the execution of a project concerned with the volume-optimisation of an inductive storage supply. The system is composed of a three stage energy conversion chain. A prime power source (low power) charges an intermediate storage (IS) which is characterised by its medium power delivery capabilities. Energy is then transferred from the IS to the storage inductor which is characterised by its high power delivery capabilities. When sufficiently charged, the energy is then transferred to the load. Where pulse forming is required, the inductor storage must necessarily be modular. Switching elements to control the energy flow are also required.

Work performed at Soreq, Israel, is used as the starting point. A topology variation of the XRAM topology presented by Soreq, original to this thesis, is presented and all its functioning modes are analysed. An existing volume model is analysed and expanded to incorporate heretofore unmodelled yet non-negligible considerations. The volume model generalises the effect of system modularity, sub-system technologies and allows for the incorporation of practical construction issues into the design process. The aim is to develop a 500 kJ, 80 kA, 20 kV system with a volume not exceeding 1m^3 . This volume must include the IS, storage inductor and full switch volume.

The optimisation algorithm and system topology developed in this thesis is validated through the construction and testing of a 1.2 kA, 2.5 kV 4 module prototype.

A potential full ratings system, composed of contemporary device technologies and exhibiting a volume of just over 0.8m^3 , is proposed.

OPSOMMING

Millisekonde pulsformingsnetwerke, soos toegepas op elektrotermies-chemiese laste, val in die <1 MJ energievlak. Die energievereistes van hierdie tipe las vereis gespesialiseerde kragbronne wat die gestoorde energie in verskillende stadiums aan die las beskikbaar stel. Tans word kapasitiewe stelsels gewoonlik vir toepassings wat minder as 1 MJ energie benodig gebruik. 'n Nadeel van hierdie stelsels is egter hulle relatiewe lae energiedigtheid. Vir toepassings waar lae volume van belang is, moet alternatiewe metodes ondersoek word.

Pulskragbronne wat van 'n induktiewe energiestoor gebruik maak vorm 'n deel van die klas van statiese kragbronne met hoë energiedigtheid.

Hierdie tesis handel oor die optimering, in terme van volume, van 'n induktiewe pulskragbron. Die stelsel bestaan uit drie stadiums, wat die energie van een vorm na 'n ander omskakel en sodoende die vorm van die puls wat aan die las gelewer word, beheer. A lae-drywing primêre kragbron laai 'n medium-drywing intermediêre energiestoor. Energie word dan van die intermediêre energiestoor na 'n hoë-drywing stoorinduktor oorgedra. Nadat die induktor volgelaai is, word die energie aan die las oorgedra. Indien pulsforming benodig word, kan van 'n modulêre induktor gebruik gemaak word. Vaste-toestand skakelelemente word gebruik om die energievloei te beheer.

Navorsing wat by Soreq, in Israel, uitgevoer is, word as die vertrekpunt vir die studie gebruik. 'n Verandering aan die XRAM topologie word voorgestel en die werking daarvan word in detail geanaliseer. 'n Bestaande volume model word ondersoek en uitgebrei om 'n aantal nie-weglaatbare verskynsels in aanmerking te neem. Die nuwe volume model maak voorsiening vir modulariteit, die effek van substelseltegnologie en 'n aantal praktiese oorwegings wat in die ontwerp van die stelsel 'n rol speel. Die finale doel is om 'n 500 kJ, 80 kA, 20 kV stelsel in 'n volume van 1 m^3 in te pas. Hierdie volume van 1 m^3 moet die intermediêre energiestoor, die stoorinduktor, asook die skakelaars, bevat.

Die optimeringsalgoritme en stelseltopologie wat ontwikkel is, word eksperimenteel deur middel van 'n 1.2 kA, 2.5 kV, 4 module prototipe geverifieer.

Laastens word aangetoon hoe 'n finale stelsel, gebaseer op huidige skakelaartegnologie, met 'n totale volume van 0.8 m^3 moontlik in die toekoms ontwikkel kan word.

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GLOSSARY

Abbreviations

PEG	Power Electronics Group of Stellenbosch University
PFN	Pulse forming network
(SP)ETC	(Solid propellant) electro-thermal chemical
ET	Electro-thermal
EML / EM	Electromagnetic launcher
EMI	Electromagnetic interference
OS	Opening switch
CS	Closing switch
P(E)OS	Plasma (erosion) opening switch
VS	Vacuum switch
VI	Vacuum interrupter
RAG	Rotating air-gap
HVF	High-voltage fuse
(HV)IGBT	(High-voltage) insulated gate bipolar transistor
NPT / PT	Non-punch through / Punch through
BJT	Bipolar junction transistor
GTO	Gate turn-off thyristor
(I)GCT	(Insulated) gate commutated thyristor
MCT	MOSFET controlled thyristor
MAGT	MOSFET-assisted gate-triggered thyristor
MOSFET	Power field effect transistor
SCR	Thyristor
D_x	Generic diode x
C_x	Generic capacitor x
L_x	Generic inductor x
S_x	Generic switch x
MOV	Metal oxide varistor
SiC	Silicon carbide
XRAM	Inverse of the MARX generator
MAPPS	Mega-ampere pulse power supply
AEC	Atomic Energy Corporation

HTSC	High-temperature superconductor
HPG	Homopolar generator
SMES	Superconducting magnetic energy storage
IS	Intermediate storage
JRC	Jellyroll coil
PCC	Pancake Coil
FEM	Finite element method
ESR	Equivalent series resistance
ESL	Equivalent series inductance
System parameters	
λ_r	Volume ratio IS_{VOL} / L_{VOL}
VOL_{TOT}	System volume excluding switch volume; $IS_{VOL} + L_{VOL}$
\mathcal{E}_{SOREQ}	Parameter representation used in Soreq's volume model
α	Parameter representation used in the continuous volume model
η_{IS-L}	Front-end transfer efficiency
η_{L-Load}	Back-end transfer efficiency
η_{DC_PAR}	Back-end transfer efficiency for system parallel discharge taking only DC losses into account.
η_{DC_SER}	Back-end transfer efficiency for system series discharge taking only DC losses into account.
N_S, N_P	Dummy variables for IS parallel and series units used in discrete volume model
n	System module number
t_{CH}	Front-end charge time
t_{Const}	Front-end time constant
t_{rat}	Ratio of t_{CH} / t_{Const}
t_d	Back-end discharge time
I_{REQ}	Required front-end charge current
E_{s0} or E_{STORED}	Total stored energy in inductor
$E_{L_ESR_TOT}$	Energy dissipated in the ESR of the storage inductor

E_{Q_COND}	Energy dissipated in the switch during conduction
E_{sa}	Energy stored as a magnetic field in the air
E_{sm}	Energy stored as a magnetic field in a conductor
k_{Ω}	IS and inductor ESR ratio modifier
ppm	Pulse per minute
IS parameters	
S_{BP}	Battery peak power
S_{ISP}	IS peak power
s_{BP}	Battery power density
I_{SC}	Short circuit current
$BATT_I$	Battery unit short circuit current
$BATT_V$	Battery unit open circuit voltage
$BATT_{ESR}$	Battery unit ESR
$BATT_{VOL}$	Battery unit volume
IS_{ESR}	Intermediate storage internal resistance
IS_{VOL}	Intermediate storage volume
IS_V	Open circuit IS voltage
Inductor parameters	
$M_{p,q}$	Mutual inductance of inductors p and q
\mathbf{M}_p	Generic characteristic inductance matrix used for general calculation purposes. Square with order p .
\mathbf{M}_n	Characteristic inductance matrix of an n -module inductor.
\mathbf{B}_p and \mathbf{B}_n	Square ones matrix of order p or n .
k_C	Coupling factor
\mathbf{r}_{obs}	Observer vector with components (x,y,z)
λ_f	Flux linkage
δ	Inductor conductor diameter
N	Inductor winding number
τ_i	Inductor time constant L_{ST} / L_{ESR_TOT}
\mathbf{B}	Magnetic field density; vector or scalar
\mathbf{H}	Magnetic field intensity vector composed of (H_x, H_y, H_z)
L_{ST}	Inductance value of storage inductor in full series

	connection
L_{ESR_TOTAL}	ESR value of inductor in full series connection
L_{VOL}	Full inductor volume
L_{ESR_X} or L_{ESR}	ESR of inductor of module n
L_{X_P}	Parasitic inductance associated with x
L_{metal}	Inductor material
L_{eff}	Inductor volume modifier
Switch parameters	
Q_X	Generic silicon switch X (usually a number or letter reference)
Q_I	Switch unit maximum current
Q_{VOL}	Switch unit volume
Q_{VOL_TOT}	Total switch volume
Q_V	Switch unit voltage hold-off capability
Q_{V_ON}	Switch unit on-state voltage
C_Q	Individual switch snubber capacitance
C_{SNUB_x}	Total switch x snubber capacitance
C_{COM}	Compound snubber capacitance
I_C	Collector current
V_{CE}	Collector-emitter voltage
t_{off}	Total turn-off time for a switch
E_{off}	Energy dissipation in a switch during a single turn-off cycle
P_{cond}	Conduction power losses
T_j	Temperature. Subscript is subject specific; j is for junction.
ΔT_{jc}	Temperature difference. Subscript is subject specific; jc is for junction to case.
R_θ	Thermal resistance. Subscript is subject specific.
Load parameters	
I_P	Initial current in an ETC load
R_P	Initial resistance of an ETC load (at peak current)
k_{load}	Lumped parameter representing capillary geometry effects
R_{cap}	Non-linear resistance of capillary

α_{ETC}	Constant used in ETC load characterisation
R_L	Load approximation as a resistor
t_{DECAY}	Time of current decay in an ETC load

Miscellaneous	
I_{B_MN}	Minimum L_2 reverse current during the charge cycle
I_{REF}	Ratio of i_{L1} over i_{L2} at the start of the first switch transient
V_{C_PEAK}	Maximum voltage peak across capacitor C
ξ	Electric field intensity
ω	Radial speed
ω_r	Frequency in radians
Cu	Copper
Al	Aluminium
m	Material mass

Physical constants	
ϵ_0, ϵ_r	Absolute and relative permittivity
μ_0, μ_r	Absolute and relative permeability
$\rho / dens$	Material density
c	Specific heat constant
ρ_{metal}	Resistivity

CHAPTER 1

INTRODUCTION

1.1 Background

This thesis forms part of the efforts of the Power Electronics Group (PEG) laboratory of the Stellenbosch University to complete a contract to perform feasibility studies into the design and construction of a millisecond Pulse Forming Network (PFN) with certain technical specifications.

For the energy envelope in question, capacitor-based PFNs are usually employed. This technology is limited, however, in that it exhibits a particularly low volume energy density. As a result of this, alternatives have to be considered, one of which is the use of inductors as the primary storage element. If only the volume of the storage element is considered, inductor-based systems offer a superior volume energy density.

Design and optimisation of an applicable inductor-based PFN is dependant on both the applied topology's electrical functionality and full system volume requirements. Design of the system must necessarily consider both requirements simultaneously.

The glossary lists all of the nomenclature used in this report. To facilitate the understanding of the report, some concepts will now be described.

PFN : A Pulse Forming Network. This is general description for a circuit topology that can deliver an energy (or power) pulse of defined duration and shape, or pulse form.

Passive storage device : Used in this thesis to describe a device that can store and deliver but not generate energy. Inductors, capacitors and inertial storage systems fall into this group.

Active storage device : A storage device that can both store and generate energy. Batteries, generators and chemical based devices fall into this group.

Active switch : A switch that does not commute naturally but depends on externally supplied control signals.

Passive pulse shaping : Used to describe the shaping of an energy pulse through the interchange of energy through a chain of passive devices (such as a inductor-capacitor ladder, for example). Pulse compression is one example. Each stage must be capable of storing the full energy. It is therefor usually used for low energy, short pulse time systems.

Active pulse shaping : Used to describe a system that transfers energy directly from the first storage element to the load. The load shaping is performed using active switches to transfer parts of the stored energy at defined times. It is usually employed for high energy, long pulse time systems.

Modular : Used here to describe an active pulse shaping system composed of several storage units. For large energy systems, pulse forming through staged passive methods (such as pulse compression) would require excessive system volume. An active and modular system is therefor used to ensure a desirable pulse form through the sequential discharge of the discrete modules.

XRAM : This is a standard modular inductor-based PFN. The name is the inverse of MARX, which is a standard modular capacitor-based PFN topology. Further explanation is give in section 1.3.

OS,CS,Q : These stand for Opening Switch, Closing Switch and Q is a switch that can both open and close. They are all active switches. Applicable switch technologies depend heavily on system power levels, required switch times, etc. The acronym is used in order to generalise the arguments presented.

Staged energy conversion : High energy PFNs are generally composed of several active or passive energy subsystems, each one characterised by its power and energy delivery capabilities. Generally, electrical generators are high energy (depending on a fuel reservoir, for example) but deliver low power levels. A PFN requires high power delivery but usually at relatively small energy levels. Some form of staged energy conversion is thus necessary.

Prime power : Describes the low power high energy source. Usually a generator. This energy source is used to keep the medium power medium energy stage charged (in the case of a battery or electrochemical capacitor stage). The Prime power source is not included in any of the optimisation procedures.

IS : The Intermediate Source, where intermediate means between the prime power source and the actual storage inductor. It is the medium power, medium energy stage, in the case of this thesis composed of an active source of batteries.

Capacitor storage : Describes the storage of energy in the form of an Electric field between two conductive supports. The technology limits depend on the permeability of the separating medium, the breakdown voltage of this medium and the geometry of the device.

Inductor storage: Describes the storage of energy in the form of a magnetic field that is generated through a current flowing in an inductor. For an air-core inductor, the technology is theoretically unlimited. Practical issues such as conductor heating and inductor strength do play an important role, however.

Front-end : A single term describing the grouping of the IS and storage inductor stages. The terms front-end efficiency, front-end matching and front-end charge time (amongst others) are often used.

Back-end : A single term describing the grouping of the storage inductor and the load. The terms back-end efficiency, back-end matching and back-end discharge time (amongst others) are often used.

Front-end Match : Front-end matching describes the classical input and output impedance matching between the IS and the inductor. In this case, the impedance in question is the Equivalent Series Resistance (ESR) of each element.

Back-end Match : Not the power matching but the transferred energy matching. The term describes the relation between the shape of the output pulse and that of the ideal load pulse shape. It is possible to transfer energy to the load that does not do desirable work; in this case the matching is not ideal.

Subsystem : The full PFN is composed of several subsystems. These are the prime source, the IS, the storage inductor, the switching hardware and the load. The term *subsystem technology* refers to the technology group (such as batteries or electrochemical capacitors for the IS) of each subsystem. When it is clear, however, that the actual technology group has been chosen, *subsystem technology* refers to the actual battery choice, for example. The optimisation process presented in this thesis describes the optimisation of the IS, inductor and switch subsystems.

Coupled inductors : The mutual inductance between two inductors. It is possible for 3 (or more) inductors to be mutually coupled. In this case the coupling between each pair of inductors (thus for 3 inductors there are 3 pairs) can be independently described.

Balanced inductors : In this case, balanced refers to inductors that are of equal inductance values. If there are more than 2 inductors and they are mutually coupled,

balanced means that the mutual inductance between each pair is numerically equal. The term *homogenous* coupling is also used.

1.2 PFNs, energy envelopes and ETC requirements

This discussion is summarised here but is further elaborated on in sections 2.2 to 2.4. The PFN class of topologies are exceptionally varied. These can be broadly divided into millisecond and microsecond systems, and use either passive or active pulse shaping methods. Possible applications in the millisecond range fall into three distinct energy envelopes.

An ETC load falls into the lowest envelope, that requiring energy below 1 MJ. The applicable subsystem technologies are understandably sensitive to this energy requirement. Pulse forming to match the ETC load profile is not a defined field, as is evident by the sometimes contradictory documentation found in the literature. However, it is assumed in this project that a modular inductive storage system, with no extra passive pulse forming hardware, sufficiently matches the ETC load requirements. This assumption is supported particularly in [4], although this consideration is not a prime focus of this research. System design considerations are also sensitive to the level of system modularity. As will be described, a module number of 4 is considered both optimal from a design perspective and sufficient from a pulse forming perspective.

1.3 Sub-system technologies

This discussion is summarised here but is further elaborated on in sections 2.5 to 2.13. Due the high power levels required by a typical system (in the hundreds of megawatts) and the comparatively low energy levels, from a converter point of view, conventional electrical supplies are not practical to apply.

An alternative to this is to use some energy storage stage, in the form of an inductor or capacitor, which can supply a sufficient power level. Alternative methods – inertial supplies or chemical supplies – are generally not applicable to low-volume low-energy ETC loads and are not considered further. This storage stage can also be used as the pulse forming stage, using active switches to commutate quantities of energy from the passive source to the load at controlled times. The energy flow path thus goes through a number of conversion stages, as depicted in Fig. 1-1. The relative

charge or discharge times and power and energy levels are also shown; the variables referred to are discussed later in the report.

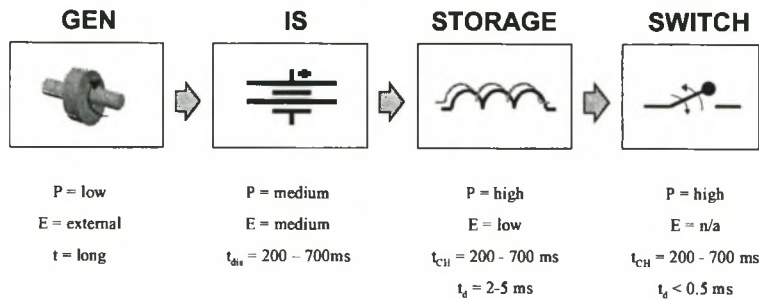


Fig. 1-1 Energy flow paths

This project uses batteries as the IS, a modular inductor as the storage element and semiconductor turn-off switches and diodes as the commutation elements. The base-topology is the XRAM topology, presented below.

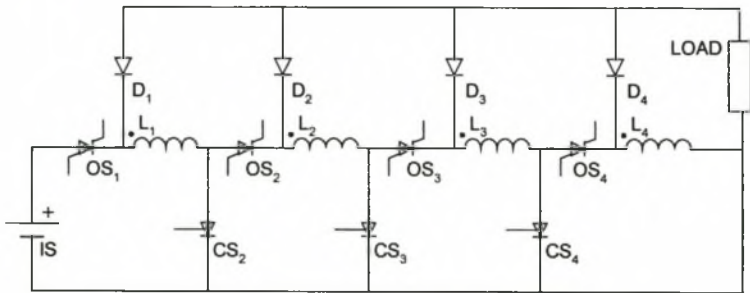


Fig. 1-2 4-Stage XRAM topology suggested by Kanter *et al.*

The name XRAM is the inverse of MARX. In a MARX generator, storage elements (capacitors) are charged in parallel and discharged in series. This allows a form of voltage multiplication. The XRAM topology performs the inverse. The storage elements (inductors) are charged in series and discharged in parallel. Thus current multiplication is achieved. The load voltage is determined by the load itself and the pulse form is determined by the natural discharge of the inductor into the load. An additional degree of freedom is possible using a modular system as limited control of the pulse form can be achieved through sequential switching of the individual modules.

1.4 Challenges posed and the role of this project

Traditionally, pulse forming networks of this order utilise capacitive storage with closing switches as the prime active switch. This technology is superior in most respects to its counterparts – particularly as it does not thermally or electrically stress

any of its sub-components and because its energy is stored in a static electric field, theoretically resulting in zero losses during its storage stage.

The single disadvantage of such systems that would warrant the use of an alternative technology is the limited energy density of capacitors; that is, the storage (and importantly as well the transferred) energy divided by the full system volume is low. Capacitive systems are as a result generally bulky. Research progression in this field in recent years has not proven sufficient to match stringent volume requirements of these systems, and as a result alternative technologies need to be considered. This project forms part of this movement.

Inductive storage methods have been researched before in the form of the XRAM topology [4][6], volume-optimised single-module systems [10][12], transformer-based systems [13][14] and even multi-megajoule systems [29]. This project re-examines these past projects and uses Refs [10] and [12] as a starting point.

This research is extended in this project to include semiconductor switches as the prime switching elements, system modularity in a volume-optimised system (not performed before) and expands the volume model to both make it more general and enable it to include previously unmodelled effects, not possible using the model proposed in [10]. Furthermore, a modified form of the XRAM topology is proposed here. It requires less volume than its standard counterpart and reduces the complexity required for system control; this topology is sufficiently analysed. A number of considerations not possible to model in this research have been highlighted; these are discussed in the relevant sections and where possible estimations are made.

The major stumbling block – recognised in these past research papers as well – is the thermal stability of the opening switches. This consideration is quantified. A product is presently on the market that to an extent matches the system requirements [38]. This system uses a flywheel, superconducting storage and superconducting switches. Mention is made of this example where relevant, although it must be stressed that this project focuses on system research using contemporary technologies with an expected prototype to product time span of 4 years. Use of superconducting technologies or even inertial storage in ETC applications requires considerations beyond the capabilities of the institution performing this research.

1.5 Project overview

Factors such as energy content, transfer efficiencies, pulse shape and system volume all play a role and are highly dependent on source technology used and energy delivery specifications.

This project aims primarily at researching modular, inductive-storage, volume-optimised, pulse forming networks for ETC applications requiring energy typically below 1 MJ at voltage levels of 20 kV, current levels of 80 kA and discharge times of around 5 ms.

To achieve this aim, a topology is suggested in the form of the modified XRAM topology, a variation of the standard XRAM topology original to this project. A complete electrical analysis is performed on the topology incorporating switch stability, discharge stage stability, relevant electrical losses, the effect of parasitics and the effect of modularization. As system volume is an important issue, a complete volume analysis is performed and optimisation procedures are drawn up. This model incorporates the effects of pulse shaping, modularization, charge and discharge efficiencies and is general to any switch and battery technology and most standard inductor technologies.

A 2.5 kV, 1.2 kA prototype is constructed that validates the topology and volume optimisation procedure.

Lastly, a novel method of active pulse shaping is presented and discussed.

1.6 Structure of this report

This chapter has briefly presented all of the important considerations involved in the execution of this thesis. A short précis of the important concepts has also been given.

Chapter 2 is included mainly as a validation for the choice final topology and subsystem technology choices that were made. No loss of understanding of the work presented in this thesis will result if the reader omits this chapter. It expands the introductory work presented in this chapter and cites relevant research projects of the last decade throughout the world. In particular, that performed in references [10] and [12] by Soreq, Israel, is relevant as it is used as a starting point in this research project.

Chapter 3 presents the standard and modified XRAM topologies and discusses the relevant structural and operational differences. A full electrical analysis of the

modified XRAM topology is performed, including analysis and stability concerns of the varied discharge states and switch transient considerations. Switch-related issues – thermal and voltage sharing concerns – are presented and analysed. Lastly, system concerns such as control, measurement and fault-situation handling are discussed.

Chapter 4 presents the volume model of the circuit and discusses the relevant volume optimisation models. The model described in [12] is presented and briefly discussed. This model is then expanded to include some general topology concerns; this is referred to as the continuous model. The limitations of this model are discussed and an alternative model is presented, described as the discrete model.

Chapter 5 discusses the important results of the volume model. Generalised volume dependencies are discussed and it is proven that the system volume is independent of the system modularity, assuming that modules are balanced (discussed in section 3.3). Lastly, a 500 kJ system suggestion is made using currently available technologies. The system has an overall volume of below 1 m³.

Chapter 6 presents the design, construction and testing of the prototype. The system is of low energy and some considerations applicable to a high-energy system are unfortunately not applicable here. This is discussed, the required model modifications are made and the general ramifications of these modifications are discussed. It is assumed that generality is not lost. Relevant construction details are given as well as some relevant results. The full power level of 1.2 kA and 2.5 kV – effectively 3 MW – is achieved.

Chapter 7 proposes a novel method of pulse forming applicable only to the use of semiconductor switches in an inductive storage PFN. The method involves pulse width modulation (PWM) of the discharge pulse to actively match the required energy profile while using a reduced module count if compared to the standard or modified XRAM topology. The general method is proposed, system stability concerns are dealt with, a rudimentary open loop fixed-frequency control algorithm is developed and promising results are documented. Reference [52] discusses an existing system that uses semiconductor switches (in this case IGCTs) to switch up to 50 kA. Thus the main associated concern with this method – that of being able to switch kilo-amperes at high speeds – is validated.

Chapter 8 closes the report with a brief summary and quantifies the contributions made by this research. In particular, the actual consideration of an inductive storage PFN for ETC applications is considered holistically and a number of

general considerations are made. Lastly, suggestions are made concerning further research on this matter.

Appendices A to G concern issues either not directly related to the ETC load but that require clarification or phenomenon-specific considerations that also require quantifying. Appendix H documents the Matlab program listings of the algorithms presented.

CHAPTER 2

PFN BACKGROUND STUDIES

2.1 Introduction

Millisecond PFNs are specialised electrical sources. A great deal of energy (in the MJ range) needs to be transferred to the load in a short time duration (in the millisecond range). A great deal of work has been performed over the last decade in an attempt to address the challenges posed by such systems. There appears to be some contention about which technologies are best suited. It is generally accepted that EMLs (Electromagnetic Launchers) are a far to midterm possibility. As a result, ETC (Electro-thermal Chemical) systems are receiving a great deal of focus. This chapter examines all the applicable systems and performs a background study on past research performed on ETC gun supplies.

Section 2.2 distinguishes between millisecond and microsecond pulses and the challenges these systems pose. Section 2.3 discusses the difference in energy requirements of the electric gun types and stipulates the place of this project. Section 2.5 gives a brief overview of the applicable sub-system technologies. Sections 2.6 through 2.12 track research and development projects world wide and discusses the relevance of this project in relation to these.

All the information used in this project is obtained either from the contractor or from public domain publications. Section 2.13 reviews applicable switch technologies.

2.2 Millisecond and Microsecond PFNs

Pulse Forming Networks, or PFNs, encompass a variety of electrical circuits. Some applications require low energies (less than 500 J) delivered in the nanosecond to microsecond range at often kHz frequencies while the other extreme requires high energies (10s of MJs) in the millisecond range and frequencies of less than $1/10^{\text{th}}$ Hz.

The applicable circuits to either are understandably varied.

For the μ s PFNs, switching losses, high voltages, pulse compression control, energy transfer mechanisms, strict dv/dt ratings, EMI and voltage isolation are important.

For ms pulses, conduction losses and thermal management, mechanical strengths, energy storage concerns and system and operator safety are the greatest challenges.

This project focuses specifically on ms pulses.

2.3 Energy Envelopes and Applicable Technologies

Energy requirements of electric guns fall into three distinct groups. McNab [1] quantifies these as shown in Table 2-1.

Table 2-1 Electric munitions specification from [1]

<i>Electric Gun Concept</i>	<i>Energy (MJ)</i>	<i>Voltage (kV)</i>	<i>Pulse Length (ms)</i>	<i>Current (kA)</i>	<i>Efficiency (KE_{out}/EE_{in})</i>
ETC (I)	0.3-0.5	12-18	1-2	10-30	50
ETC	3-5	12-18	3-4	30-50	5
EML	30-40	5-7	4-6	3000-4000	0.5
Pure ET	60-90	22-80	3-4	50-100	0.2

Three envelopes are apparent. The first encompasses energies below 1 MJ, the second energies between 1 and 10 MJ, and the third for energies over 10 MJ. For each envelope, different PFN technologies are applicable. This project caters for the design of a prototype ETC gun. Correspondence with the contractor in January 2000 established this project’s specifications as depicted in Table 2-2.

Table 2-2 Contractor ETC specification

<i>Electric Gun Concept</i>	<i>Energy (MJ)</i>	<i>Voltage (kV)</i>	<i>Pulse Length (ms)</i>	<i>Current (kA)</i>
ETC (I)	0.7	20 kV	5	80

2.4 Pulse shape requirements for an ETC load

Matching between the load and the supply is a factor requiring specific attention. This requires modelling of the load during the whole discharge transient. Kanter *et al.* [4] considers

$$R_{cap.} = k_{load} \cdot i_{cap.}^{-\frac{6}{11}}, \quad 2-1$$

to suffice where k_{load} is a parameter lumping the effects of the capillary geometry, R_{cap} is the non-linear capillary resistance and i_{cap} is the capillary current.

The natural discharge of an inductor (single module) into a capillary load can be calculated and is given in [4] as

$$i_L = I_p \left(1 - \alpha_{ETC} \frac{R_p}{L_{ST}} t \right)^{\frac{1}{\alpha_{ETC}}}, \quad 2-2$$

where I_p is the inductors peak current just before discharge, R_p is the capillary resistance at peak current, L_{ST} is the inductor value and α_{ETC} is the value $-6/11$. For a capacitive discharge profile, the same process generates the equation

$$i_C = I_p \left(1 + \frac{\alpha_{ETC}}{1 - \alpha_{ETC}} \frac{t}{R_p C_{ST}} \right)^{\frac{1}{\alpha_{ETC}}}, \quad 2-3$$

where C_{ST} is the storage capacitor value. Graphically, the discharge profiles are shown in Fig. 2-1.

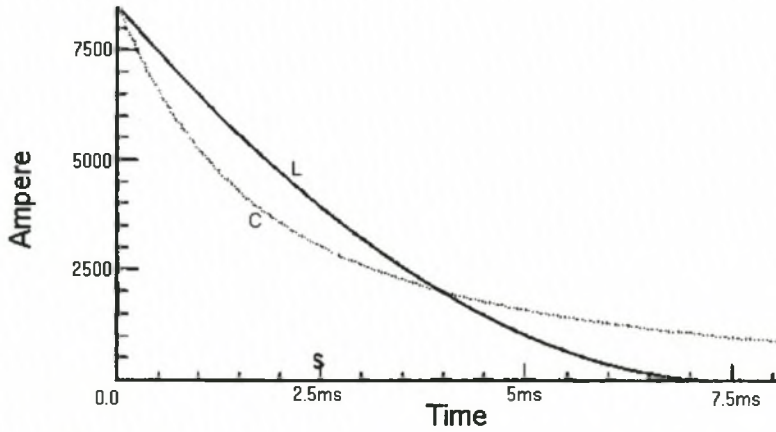


Fig. 2-1 Discharge profile for capacitive and inductive sources from [4]

From inspection of Fig. 2-1, it is observed that the discharge for the inductive storage appears almost linear, and the current reaches zero after a finite time. As a result, theoretically all the stored energy is utilized. Thus the inductive source appears more efficient than the capacitive source, and allows for a more favourable discharge profile.

However, research performed by Guyott [5] in conjunction with DERA in 1995 indicated that the optimum discharge profile was close to a half sine wave, as

indicated in Fig. 2-2. It is shown in this project that even this energy transfer form can be generated using a 4-module XRAM topology (section 6.7.4).

However, it seems that these factors are highly dependent on the quantity of energy utilised and the ETC capillary. Private correspondence with the contractor in January 2000 indicated that pulse forming was indeed required; a single module inductive element would not be sufficient.

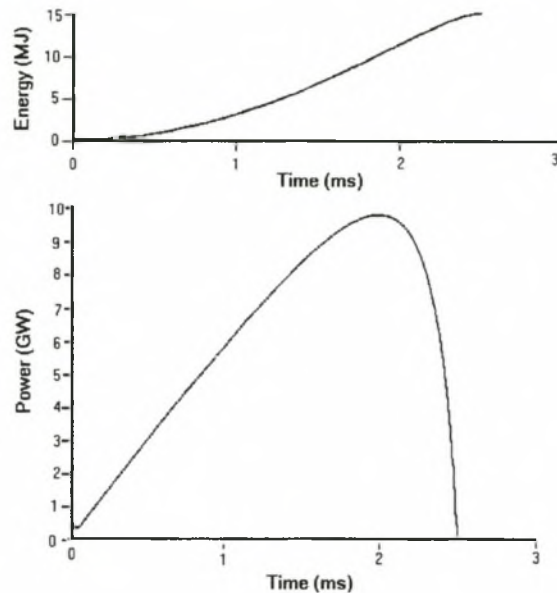


Fig. 2-2 Optimised Discharge for ETC load from [5]

2.5 Sub-system technology overview

This section provides a brief description of the applicable technologies. Sections 2.6 through 2.12 provide further detailed descriptions. This section is mostly based on research performed by McNab [2] and Gully [3] from the University of Texas, Austin. Where lacking, supplementary reference material is used but is not referred to here; complete referencing is done later in the chapter.

2.5.1 Capacitor based systems

The advantages of capacitor-based systems over the alternatives are numerous. The system has no inertial components, the capacitors can remain primed for an appreciable length of time (dependent on the specific technology) and the commutation of energy into the load is performed using closing switches. The closing switches only conduct current during the discharge phase. The primary disadvantage of capacitor-based systems is the limited energy density of the capacitors themselves.

If this were not a limiting factor, capacitor based systems would be superior to all its non-inertial counterparts. A recent publication claims a pulse-applications capacitor with energy density of 2 MJ/m^3 has been developed [48].

At the present state of the art of available capacitor technologies, however, alternative technologies need to be considered.

2.5.2 Inertial Systems

The focus on inertial storage systems has been specifically for high energies as suits the EM launcher requirements. For systems with an energy requirement below 1 MJ the advantage of inertial systems over alternatives is reduced. Of the inertial systems, the Homopolar Generator and the compulsator are possibilities.

This project is specifically focused on non-inertial supplies, however, and as a result no in-depth comparative studies concerning inertial-only systems have been performed. Flywheels are another option; however, they are considered as intermediate storage technologies as standard flywheel systems are not compatible to pulse applications if used directly.

2.5.3 Superconductor/Hyperconductor systems

The advantage of super-conductor based inductive storage systems is that energy can be stored in the inductor with no thermal loss. As a result no pre-shot priming is required. Also, importantly, the use of superconductor switches avoids the conduction and resulting thermal problems experienced using other switches. Refs [37] and [38] describe a system comprised of a flywheel intermediate storage (IS) and superconductor inductor with superconductor switches.

Hyperconductors are not true superconductors but have the advantage of not having the related material-properties problems. However, both the infancy of the superconductor field and the required peripheral hardware (even with high temperature superconductors) makes the application of superconductor-based systems, at least in the immediate future, not a feasible option.

2.5.4 Chemical based systems

Chemical systems include battery based and fuel cell based systems. Although chemical units have very high energy densities and can deliver high currents, the low power density (effectively the units low operating voltage) makes it difficult to apply

chemical based technologies to pulse power applications. However, the battery can and does form an integral part of hybrid systems as the IS.

2.5.5 Other

The Magneto-hydrodynamic generator (MHD) received a great deal of attention in the 1970's and early 80's. However, research into high-energy systems has not progressed far and the system is not generally considered as viable. Flux compressors have the disadvantage of also requiring chemical fuels or some mechanical actuation and as a result are also not considered here.

2.5.6 Inductor based systems

Inductive storage methods are superior to other non-inertial systems because of the storage element's comparatively high energy and power density. Capacitor based systems are actually composed of the capacitor as intermediate energy storage and then an inductor to shape the pulse. This inductor is capable of storing the full energy and is only a fraction of the volume of the full system.

The problems associated with inductor-only storage methods are numerous, however. Inductor storage methods can be put in two classes: the direct drive systems (inductor based) and transformer based systems.

The two technologies require different design considerations (such as load impedance matching) but the switch and IS requirements for both are the same, independent of power or energy levels or module number. However, non-unity coupling of the charge coil and the discharge coil in transformer based systems results in stored energy that is retained at the primary during commutation which must be absorbed by the switches themselves. As solid-state switches are particularly susceptible to this type of problem, direct drive systems are considered superior. Also, inter-module coupling in a coupled modular transformer based system results in restrictive discharge allowances not observed with inductor only based supplies.

2.5.7 Direct Drive inductor based systems

Direct drive inductor based systems (from now on referred to as inductor based systems) can be classed as either coupled or uncoupled systems. As pulse forming is generally required, a modular storage system is used. Coupled systems allow for higher energy storage and result in increased energy density. However, the topologies

of the two systems are the same (less the coupling relationships) and research in one is directly transferable to the other.

The XRAM topology is the most electrically compact system and is the chosen topology for this research. Fig. 2-3 shows an applicable XRAM topology.

2.5.8 Hybrid Systems

Strictly speaking, all the systems are hybrid systems as they generally require four-stage energy conversion from the prime power source to the intermediate source to the storage element and then to the load. The nature of each storage element determines its compatibility with other storage systems.

For capacitor based systems, the prime power charges the capacitors which act as the IS. The capacitors can either discharge directly into the load or more often into an inductor, which acts as the pulse former.

Ref. [37] describes a system where a prime power source charges a flywheel (the IS). The flywheel then charges a coupled 6-module super-conductive storage element that performs the energy transfer to the load and shapes the pulse.

The system applied in this project utilises a battery IS and a coupled 4-module inductive storage element.

2.5.9 Storage technology comparison

There is lack of agreement between references. Reference [3] considers a standard 1:10:100 energy storage density for capacitive : inductive : inertial. Table 2-3 shows that inductive storage has a higher density than inertial storage. This is because the magnetic field density (B) of 40T in a slow charge system is highly unlikely; the inductor itself would experience thermal problems. Inertial storage mechanisms are not considered further in this report.

Table 2-3 Energy storage mechanisms and technology comparisons [1]

<i>Device</i>	<i>Method</i>	<i>Equation</i>	<i>Assumption</i>	<i>Typical state of the art</i>	<i>Energy density</i>
Capacitor	Electrostatic	$E_{so} = \frac{\epsilon_o \epsilon_r \xi^2}{2}$	High energy density plastic film	$\xi_{op} =$ 400V/m; $\epsilon_r = 10$	7
Rotor	Inertial	$E_{so} = \frac{I_M \omega^2}{2}$	High-speed composite/ conductor rotor	$\rho =$ 1500kg/m ³ $v = 600$ m/s	135
Inductor	Magnetic	$E_{so} = \frac{B^2}{2\mu_r \mu_o}$	High field air-core	$\mu_r = 1$ $B = 40$ T	640
Battery	Electrochemical		LiMS at 480°C	1.72 V / cell	4000
Flux Compressor	Chemical		High Energy density materials	Few eV / bond	5000- 10000

2.5.10 Turn-Off Switches

Capacitor based systems allow an inductor to be charged by the capacitors; the inductor then freewheels through passive switches (diodes) into the load when the capacitor's current attempts to change direction (effectively a simple resonant circuit).

With inductor-only based switches, batteries replace the capacitors. The batteries have a lower voltage and thus the system requires longer priming times. Furthermore, the batteries' voltage does not fall to zero and no current reversal takes place; as a result the inductor's current needs to be 'force commutated' into the load. This is performed using opening switches. A number of difficulties are involved.

The applicable opening-switch technologies are classed as non-solid-state and solid-state.

2.5.11 Non Solid-state Turn-off Switches

This covers magnetic switches, mechanical switches (such as contactors or breakers), explosive switches and plasma erosion switches (or POS or PEOS switches). Ref. [53] documents research conducted under this project and discusses a number of these methods.

The advantage of non solid-state switches is that they allow high current conduction and are in general very robust. The disadvantage of these switches is their peripheral complexity (in some cases), their size and their slow and sometimes unpredictable switching behaviour.

Hybrid switches using a mix of non-solid-state switches and solid-state switches is an option that has found application in a number of instances. Effectively, the non solid-state switch conducts the charging current and passes the current into the solid-state switches just before commutation. This has the advantage of not allowing the thermal conduction stage problems solid-state switches would experience to occur (a serious problem) and reduces the commutation problems non-solid-state switches experience.

However, a large volume advantage should be gained if the non solid-state switching stage is omitted.

2.5.12 Solid-state Turn-off Switches

Gate turn-off thyristors (GTOs), MOSFET-commutated thyristors (MCTs), Gate commutated thyristors (GCTs), MOSFETs, Insulated Gate Bipolar Transistors (IGBTs) and force commutated thyristors are all options.

Traditionally, GTOs have been used in high current applications due to their high power ratings. However, GTOs require extensive gating circuitry (at least 20% device rated current for the driver) and are thus progressively being replaced by alternative switches.

MCTs have fallen out of production.

Research on the application of IGBTs to PFNs should be transferable to GCTs if the devices prove superior in the long run. Ref. [52] discusses the construction of a very-high current turn-off switch using a matrix of GCTs.

MOSFETS are extremely fast devices but are limited to low-voltage applications.

IGBTs are currently the chosen devices for most power electronics applications due to the high power ratings of the devices, fast switching speeds and very simple voltage-based gating circuitry. The devices do not have the same power ratings as GTOs but the extensive international research on these devices allows for a rapid rate of development. At the time of device selection for this project, 3.3 kV devices were the best available. A year later, 6.5 kV devices are available. The devices are still rated at comparatively low currents, however, and this continues to be a problem.

The forced commutation of thyristors is also an option, but the peripheral hardware requirements render the method inapplicable. With an eye on future improvements to the IGBT range, it is considered best to research the application of these devices to millisecond pulse power applications.

An added advantage of solid-state switches over the alternatives is the extremely fast switching times; commutation can occur in under 1 μ s. This means that the switching losses are almost negligible (for ms pulse applications, conduction losses are a distinct problem for the switch itself). As a result, a great deal more freedom is allowed during the pulse forming, as it may be viable to apply some type of pulse width modulation to the energy pulse at no extra system cost.

The difficulties involved in applying solid-state switches are numerous, however, as the switches are sensitive to thermal stresses and over-voltages. These factors are discussed in section 3.10.

Alternative solid-state switch materials have been receiving a great deal of attention. In particular, silicon carbide. SiC is a very hard material and as a result has a higher thermal conduction and can conduct a much higher current due to possibly improved thermal management within the device. Predictions of SiC IGBTs with 15 times better current carrying capabilities have been made [57]. Manufacturers such as ABB appear interested in SiC [58].

2.6 Soreq, Israel, and Direct Drive Inductive Storage Systems

2.6.1 Introduction

Research and development on direct drive inductive storage methods for ETC applications has been led by the Soreq Nuclear Research Centre in Israel. McNab and

Gully consider the challenges posed by inductive storage methods as too severe. This is reflected in the work performed in the respective areas (discussed later).

The main personalities in the Soreq team are M. Kanter, Z Kaplan, R. Cerny, A. Pokryvailo, N. Shaked and D. Melnik. The work by this group shall be referred to as Kanter *et al.* Since 1989 the group has documented their progress through a number of international publications in the IEEE Magnetics transactions and other conference proceedings. References [4],[6],[7],[8],[9],[10],[11] and [12] trace the development of an inductive storage PFN from its 10 A XRAM beginnings in 1989 [6] till a prototype with energy storage of 0.5 MJ and volume of less than 700 l in 1997 [12]. The work covers most of the important issues concerned with inductive storage. However, pulse forming and modularity are not considered in the final system.

2.6.2 Year 1989 [6]

In 1989 Kanter *et al.* suggested utilisation of the XRAM topology as shown in Fig. 2-3. Kanter *et al.* constructed two circuits. The first was a 10 A MOSFET based system used to examine the operation of the system. The second was a 3-module GTO based system (with coupled storage elements). The second circuit was charged up to 500A priming current. Programmed discharge of the elements to ensure desired power discharge profiles was analytically demonstrated for an uncoupled n-module system. This is not repeated in this project. The focus of the 1989 paper is specifically on the matching of the source to the load.

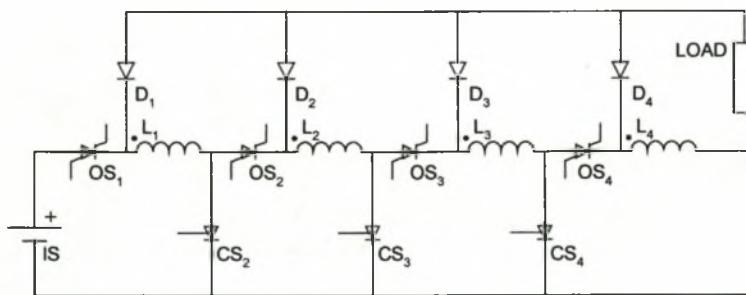


Fig. 2-3 4-Stage XRAM topology suggested by Kanter *et al.*

It appears that problems associated with this topology were not as yet an issue. A vacuum interrupter and GTO hybrid switch was suggested but not implemented.

2.6.3 Year 1992 [7]

The work of 1989 was continued and a 10 kA load current GTO based 4-module system was constructed. In specific, a capacitive IS was implemented with a charge voltage of 1800 V. Some switch overdriving is also performed. The focus of the paper is on the electrical operation of the GTO, the energy stored vs. transferred ratio (although not in depth) and current balancing between modules. No specific volume optimisation was performed. It appears that even at this stage a number of the primary problems had not been recognised (conduction losses and IS requirements). All of these considerations are revisited in the description of this project's functioning.

2.6.4 Year 1995 [10]

Kanter *et al.* examines a number of relevant considerations. In particular, a battery (IS) inductor optimisation, discharge efficiencies of the inductor, switch losses and fringing field problems are considered. The first two are revisited in later publications and are not discussed here. However, the optimisation considerations focused primarily on the relationship of the battery power density (effectively its W per litre ratio) to the allowable mechanical stress of the inductor in question; this aspect is not discussed further in this paper as it is discovered that the volume minimum is found appreciably below the failure level of the inductor.

The switch loss parameters are drawn up and it is calculated that for a tolerable loss of 10% of the stored energy in the switch itself, the switch can close in anything up to 500 μ s.

In order to deal with the problem of fringing fields, Kanter *et al.* suggests a toroidal-like structure composed of cylindrical coils placed head to tail in a circular pattern. It is observed that 4 such modules provide for sufficient fringing field reduction (a further increase in number does little to help). It is stated though "... at an energy level of several hundreds of kJ, a preference should be given to a (single) Brooks coil. In experiments (using a Brooks coil) we never encountered EMI that could not be coped with by conventional methods".

2.6.5 Year 1996 [8][9]

In [8] Kanter *et al.* implemented a Hybrid switch as documented in Table 2-4 in an attempt to meet the rigid requirements posed by a long conduction time for a high current.

Table 2-4 Hybrid switch statistics

Conduction Time	0.2-0.4s
Peak Breaking current	Several tens of kA
Hold-off Voltage	Several kV (up to 3 kV)
Opening Time	< 500 μ s

Kanter *et al.* utilises a hybrid switch composed of a vacuum switch (VS), a thyristor (SCR) and a high voltage fuse (HVF) as shown in Fig. 2-4. The VS acts as both the main turn on and turn off switch with the SCR / HVF arm as a commutation assist. The VS closes and charges the storage inductor. Charge times from 35ms to 250ms were considered. When sufficiently charged, the VS attempts to commutate. When the VS voltage reaches a pre-defined value (typically 10 V), the SCR is initialised and the HVF arm conducts. The HVF assumes the VS current for a duration long enough for re-establishment of the dielectric strength in the VS. This is typically 2-3 ms but 0.5 ms was attempted and proved successful.

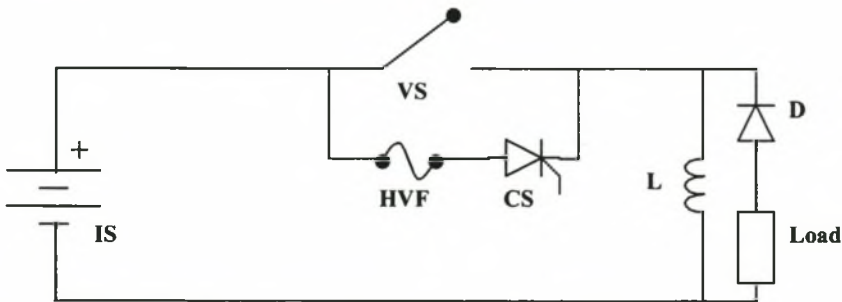


Fig. 2-4 Kanter *et al.* hybrid switch [8]

The research was focused mainly on the HVF and a number of different structural parameters were experimented with. The fuse is naturally destroyed after each firing.

The advantage of using the VS / SCR / HVF combination is the switch’s high current capability. The switch was rated for up to 80 kA. Switch volume is not documented.

In [9] Kanter *et al.* examined the discharge efficiency of cylindrical storage coils. In particular, the Brooks coil (single layer, Brooks dimensions) in a jellyroll coil (JRC) and pancake coil (PCC) configuration were examined. The argument deals with the observation that the discharge efficiency, defined as the ratio of the energy

transferred to load to the energy stored in the coil, is a great deal lower than can be described by either DC losses or skin effect losses. This is attributed to the relaxation of a magnetic field into a conductor and the rate at which this relaxed field can reach zero. The relevant time constants are considered (discharged energy to energy retained in the coil) and the dependence of the transferred energy on winding configuration is considered qualitatively and for two cases transfer efficiency is quantitatively determined. A finite element (FEM) package was utilised. Some in depth analysis was performed that does not have direct relevance on this project but it is mentioned here for the sake of completeness.

The FEM tests performed were on single layer coils using plate conductors. As a result the field and current distribution throughout the conductor can vary considerably depending on the spatial arrangement of these conductors, the exciting current and the resulting H-field. The analyses performed are thus highly dependent on these factors and a generalisation is not applicable.

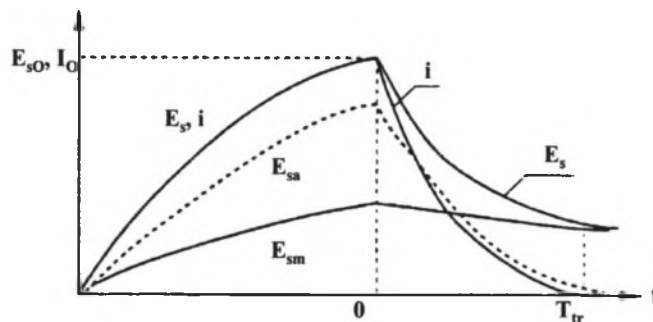


Fig. 2-5 Kanter *et al.* energy storage comparisons [9]

As observed in Fig. 2-5 E_{s0} is total energy stored in the inductor, i is the charge and discharge currents, E_{sa} is the energy stored outside of the conductors in the air, E_{sm} is the energy stored as a magnetic field inside the conductors and E_s is the transferred energy. As can be observed, the full energy stored is not totally transferred. Part of the energy is effectively stored within the conductor. This is because inside the conductor there are circulating currents that result in a net zero current but still store energy.

The relevant time constants are clearly observed; the energy stored in the conductor-part of the inductor is dissipated within the conductor and thus results in a slow dissipation rate and duration while the energy stored in the air is dissipated in the load at a faster rate. Thus there are considerable losses within the inductor itself.

Assuming that the energy is stored in a DC H-field, full penetration of the H-field has occurred (full relaxation), and element superposition (as described in 4.2.5) is valid. During the discharge cycle, it can be assumed that the self or externally excited field within the conductor does not contribute to the transferred energy and is fully dissipated in the conductor itself. Firstly, it becomes clear that a distinct difference exists between short charge and long charge coils and secondly a worst case transfer efficiency for particular spatial configurations and charge times using this assumption can be calculated.

2.6.6 Year 1997 [11][12]

These two publications describe the construction of the same system from different perspectives. The system is rated at 5 MW, 300-400 kJ, 50 kA and 10 kV. The first paper focuses on the construction of the IS. In particular, the following points are considered:

1. The charge cycle is characterised by power-matching between the inductor ESR and battery/buswork ESR.
2. The battery ESR and buswork parasitics are considered and issues such as balancing between parallel strings are considered. Mechanical issues as concerns the battery bank are also dealt with.
3. A Siemens vacuum circuit breaker is utilised as the closing switch.
4. For low current experiments, a GTO-based switch with ratings of 4 kA, 4 kV was used. For the high current experiments, an explosive breaker rated at 100 kA, 10 kV, 0.1 ms was used.
5. A number of ETC-load experiments were conducted, showing that a single module inductive storage element provided sufficient performance.
6. Full system optimisation as concerns IS and Inductor optimisation was considered from an energy storage perspective. Preliminary tables were drawn up weighing shot repetition rate, battery energy storage content and system volume concerns. This consideration is not approached in this project other than to consider transfer efficiencies.

Ref. [12] is a continuation of the former reference and is the primary reference material for this project. Most of the difficulties discovered in this project are considered here. Table 2-5 documents their system statistics.

Table 2-5 Kanter *et al.* system statistics

<i>Parameter</i>	<i>Value</i>
Conduction time	0.4 s
Peak (breaking) current	60 kA
Hold-off voltage	6 kV
Opening time	< 500 μ s
Pulse repetition rate	6 – 10 ppm

2.6.7 Summary

The following points are of interest:

1. A detailed volume optimisation procedure for battery based inductive storage pulse forming networks is discussed. In particular, factors taken into account are the mechanical strength of the inductor, system charge time, transfer efficiency, switch losses and stored energy.
2. Switch loss parameters (as per [10]) were incorporated into the design. A turn off time of less than 500 μ s is considered sufficient to ensure not more than 10% loss in the switch itself.
3. The coil discharge efficiency is incorporated into the optimisation (as per Ref. [9]).
4. Matching to the ETC load is again considered and a single module system is considered sufficient.
5. The opening switch is that discussed in Ref. [8]. As a summary, Kanter *et al.* considers “our preliminary design showed that for an 0.5 MJ tank based OS employing commercially available components will occupy 0.2 – 0.3 m³”. No reference to the makeup of this switch is made.
6. System extras such as current protection, over-voltage protection, buses, auxiliary contacts and the battery charge (or prime power) are all considered.

No further publications from Soreq were found. Although this paper specifically is the primary reference used in this project, the following points not addressed, or insufficiently addressed, can be listed.

1. Over-voltage protection as concerns the OS is not considered sufficient. Stray inductances are considered in the battery bank design in Ref. [11] but not taking

the switching transient fully into consideration. The utilisation of MOVs for over-voltage protection is also re-approached.

2. System modularity. Kanter *et al.* consider a single 0.5 MJ element to be sufficient. Other references, and in particular correspondence with DERA, consider otherwise.
3. The OS detail provided is not sufficient. The experimental data provided in the paper is not from a volume-optimised system. The predicted 0.3 m³ 60 kA switch is not utilised. It has become clear through the course of this project that the volume optimisation is most dependent on the volume of this switch. This factor should be more explicitly quantified.

2.7 Dayton, Ohio, USA, and MAPPS technology

2.7.1 Introduction

Transformer based inductive storage supplies have not found much application in ETC installations. The advantages of transformer based supplies are that, firstly, load-source matching can be easily performed and secondly the primary, or charge, coil can be of a large inductance and a low current, reducing the current demands of the prime power source and reducing thermal loss in the charge coil itself.

D.E. Johnson and N.D. Clements of the IAP Research centre in Dayton, Ohio, USA, researched the application of a hyperconducting transformer based PFN for ETC applications. The first recorded reference (not used here) to this research was in 1985. Further research was documented in the IEEE transaction for Magnetics (mostly) in the years 1989 to 1991. No reference to the continuation of the research was found. In particular, five references are used, [13], [14], [15], [16] and [17]. The transformer used was rated at 1 kA primary, 100 kA secondary. The MegAmpere Pulsed Power Supply (MAPPS) technology is described and preliminary results are documented. Of importance is the motivation provided, included below.

“... one application alone makes the [MAPPS] technology worth developing: low temperature cryogenics.”

2.7.2 Year 1989 [13]

The MegAmpere Pulsed Power Supply (MAPPS) technology is introduced in this paper and preliminary results are documented. The MAPPS technology is based on

hyperconducting aluminium, which is super-pure aluminium (purity levels were not documented) cooled to liquid nitrogen temperatures, or 77K.

The advantages of this system are that the prime power need not deliver a high current (for the transformer side) and that thermal losses within the charge coil are minimal (due to the cryogenics). IAP claims that superconducting inductors applicable to EM and ETC applications would be unable to store the currents required, mainly due to current density saturation, H-field quenching of the device and thermal contamination of the connecting leads.

Section [38], documenting research conducted elsewhere, discusses later technologies that apparently overcome these problems.

IAP considers the low current primary transformer based supply as a solution to these problems. Fig. 2-7 shows a photograph of the installation.

Fig. 2-7 and Fig. 2-8 show a schematic and a photo of the same system. In Fig. 2-8, (A) is the GTO, (B) is the Vacuum Interrupter (VI), (C) is the diode stack and (D) is the bleed resistor. The switch was rated at 1 kA. The system was rated at storing 20 kJ and delivering 100 kA. Due to switch failure, a level of 460 A (primary side) was the maximum achieved in this series of experiments. The IS required for a transformer based supply needs to be of a high voltage; the power levels required (V times I) are the same as the direct drive system for a set energy storage. The GTO was used to extinguish the plasma column that develops when the VI, pneumatically controlled, is pulled apart approximately 6 mm. The function of the MOV (metal oxide varistor) is to ensure that the reflected voltage is placed across the VI and not the GTO. It is clear in the publication that the designers were not experienced in the use of the GTOs; the resulting failure of the device at less than half rating is possibly indicative of this.

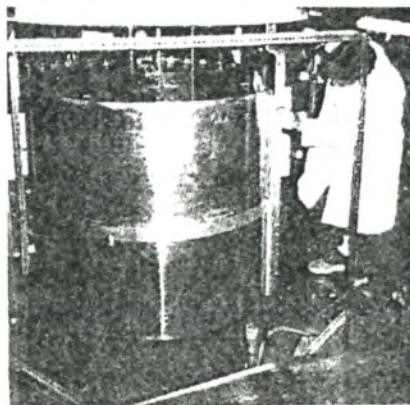


Fig. 2-6 MAPPS system photo [13]

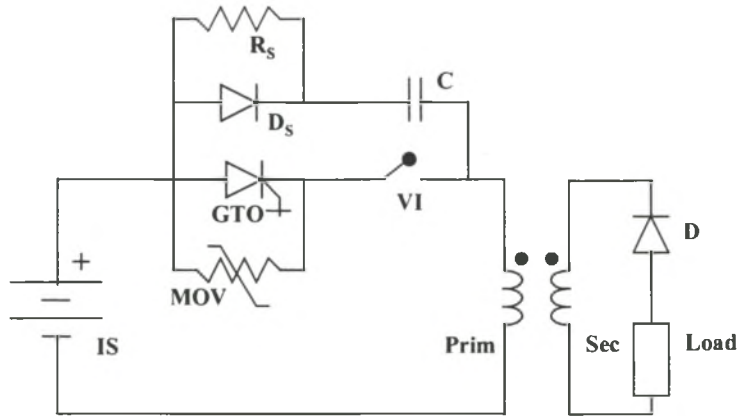


Fig. 2-7 IAP MAPPS hybrid switch [13]

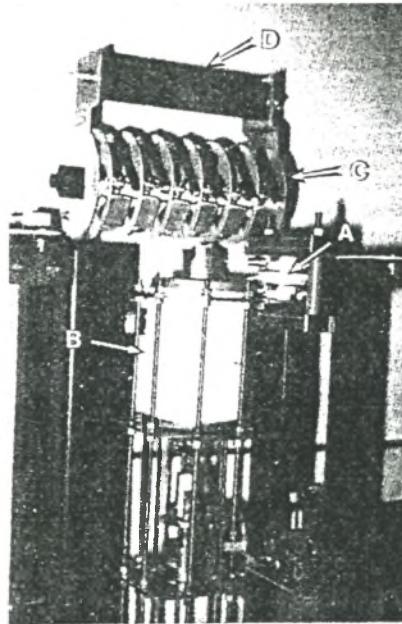


Fig. 2-8 MAPPS switch photo [13]

2.7.3 Year 1990 [14]

This paper focuses on the design of 5 MJ 1 MA MAPPS system based on research conducted with the 100 kA model in [13]; no record of the system's actual construction was found. The proposed circuit is intended for EML requirements. The device is reportedly cooled to liquid hydrogen temperatures and requires a primary current of 10 to 50 kA; the opening switch needs to conduct this current continuously. The paper focussed on the coupling co-efficient, length to turns ratio and maximum internal strain of the device. A sizing model – aimed to minimise inductor mass and volume – was drawn up.

The research conducted here takes no account of the peripheral requirements that would be understandably extreme. The opening switch, refrigeration and IS requirements are not mentioned. No mention is made on the reflected voltage on the primary. Coupling losses – that need to be absorbed by the switch – were mentioned in the last report but not in this report. Ref. [17] considers the switch requirements further.

Table 2-6 5 MJ MAPPS statistics

<i>Parameter</i>	<i>Value</i>
Transformer Mass	325 kg
Radius	0.1 m
Length	0.2 m
# turns primary	56.7
# turns secondary	2.8
Stored energy	5 MJ
Peak Sec. Current	1 MA
Peak secondary voltage	2 kV
Winding density	0.95
Coupling co-efficient	0.99

The system of Table 2-6 was not constructed (at least there is no reference to the construction of the final system).

2.7.4 Year 1991 [15][16][17]

Three publications dealing with the relevant system aspects of the 5 MJ, 1 MA system were published. The main focus is placed on the turn-off switch and system mass minimisation; turn-off switch volume is related to the coupling of the primary and secondary as displayed in Fig. 2-9. Three opening switch configurations were considered. In the two hybrid switches, the VI is to provide for voltage hold-off, the GTO is to ensure commutation of the switch, the MOV is to ensure that the reflected voltage from the load (that is, load voltage times winding ratio = 40kV!) falls across the VI and not the GTO and the capacitors are to perform both over-voltage snubbing and absorption of the coupling losses. The GTO only switch suggested has a volume equivalent to that of the Hybrid switch.

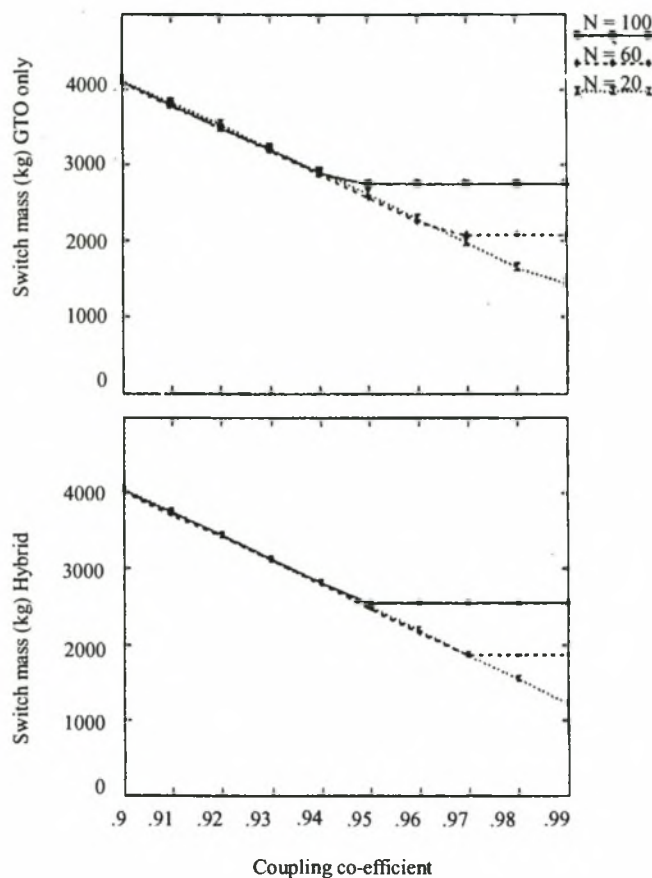


Fig. 2-9 Switch volume comparisons for coupling co-efficients of MAPPS [15]

Switch volume dominates the full system volume for a coupling of less than 0.999. As the coupling is reduced, more energy needs to be absorbed by the switch. This is performed by the snubber capacitors (the snubber voltage must not exceed the VI breakdown of just over 40 kV). These capacitors, for both the GTO-only and Hybrid system constitute about 75 % of the full switch rating.

It is observed that at a high (yet reasonable) coupling, the capacitor volume flattens out. The transformer volume (for couplings of less than 0.99) remains relatively constant at about 400 kg. The number N is the turns ratio. Energy storage values and IS specifications are not supplied in the references. It is observed that the switch volume completely dominates the system volume.

2.7.5 Summary

The advantages of using transformer-based supplies are listed below.

1. If the IS is incapable of delivering sufficient current, some type of magnification needs to be implemented. This can be done using a modular direct drive approach (such as the XRAM topology) or a transformer stage.
2. The Primary effectively only establishes a H-field (stored energy) in the flux linkage paths of the load (secondary) coil. As a result, a great deal of versatility is available to the designer, as only the secondary needs to match the load; the primary side can easily be tailored to match the front-end source.

The advantages of using hyperconductor-based storage are:

1. Over superconductor storage – although hyperconductors do exhibit losses, the structural strength of hyperconductors over superconductors far outweigh the disadvantage of a small thermal loss.
2. The current can be stored for a great deal of time.

The disadvantages of the transformer technology are:

1. Coupling losses need to be absorbed by the switch.
2. The primary (charge coil) side voltage is extremely high when compared to the direct drive alternative. For ETC applications where the load side experiences a 20 kV rise, the primary needs to hold off the reflected voltage of n times 20 kV. To reduce the reflected voltage, the winding ratio can be reduced but this also reduces the coupling coefficients and volume and mass advantages. Although the switch power requirements of a transformer based and direct drive system are the same (independent of module number and excluding additional non-unity coupling concerns), it is considered better to keep the voltages as low as possible to reduce isolation problems.
3. Modularity for transformer-based systems requires either uncoupled modular systems (which results in reduced system energy density) or else dummy-load assisted discharge of coupled primaries needs to be implemented; neither option is considered superior to direct drive systems.
4. IAP claims that “If current is available from the generator at the required load current, energy storage is accomplished much more simply in a simple inductor”. The use of a modular direct drive system in the XRAM topology is also effective in allowing for current multiplication.

The use of a transformer in a high-energy inductive storage system should be avoided if possible. Where installations already exist that can only cater for systems where some impedance matching is required then the transformer is the best. If an IS is available that can deliver the required current levels, the direct drive system is the better.

Where volume optimisation is required, it appears that with coupling requirements aside, the direct drive system and the transformer based system are very similar.

However, factors such as coupling losses, possible peripheral requirements, modularity problems (best implemented with a direct drive topology) and circuit simplicity result in the direct drive system being the preferred technology.

2.8 The University of Texas at Austin

2.8.1 Introduction

A variety of research has been performed at this institution. Documentation is recorded from 1991 to 1997.

The lead figures are I. McNab (who appears jointly affiliated to the University and Maxwell laboratories), J.H. Gully, R.C. Zowarka and W.F. Weldon. The research covers holistic ETC system technology discussions [2][3], Homopolar generator and explosively operated turn-off switch technology [17] and alternative inductor design considerations [18]

2.8.2 Year 1991 [3] [18]

In 1991 Gully performed an overview research into the various applicable technologies to electric guns. The focus was on all types of electric guns and all types of storage systems, including capacitive, inductive, inertial and chemical systems. No particular recommendations were made.

Research into an explosively operated turn-off switch for an HPG supply at the Balcones installation is performed (no reference to this installation could be found). Operation of this supply is similar to the multi-module XRAM topology suggested by Kanter *et al.* but utilises HPGs in place of a battery IS. The installation is rated at 60 MJ, 6 units, each a 10 MJ homopolar generator and requires a robust opening switch. The switch is destroyed at each commutation.

Specific research into the development of a high energy, toroidal like multi-element inductor was performed. The inductor is applicable to a HPG or Battery IS based systems. Again, system is rated at very high energies applicable to EMLs and is not directly applicable to ETC systems although the toroidal design approach is worth considering. It is a more formal approach to that proposed by Kanter *et al.* and reduces fringing field effects considerably. However, the units are not Brooks-shapes and as a result the focus is not on volume optimisation.

2.8.3 Year 1997 [1]

This is the main reference considered in this report as concerns a holistic system design approach. At this stage the relevant technologies are more mature and the Homopolar generator appears to have fallen out of favour.

2.8.4 Summary

It appears that the University of Texas is closely affiliated to the military installations under the ARL and US Air Airforce as some of their work appears referenced to in publications from these institutions. McNab and Gully in specific provide for quantitative technology comparisons that are useful in a holistic system design.

2.9 US Army Research Laboratory, Aberdeen proving ground, MD and Fort Monmouth, NJ, USA

2.9.1 Introduction

Two main centres under the ARL were/are active in electric gun research. The first at Aberdeen Proving Ground, MD, seems to be focussed mainly on capacitive storage, multi-module ETC (or SPETC as referred to here) LC shaping circuits. It appears that no volume optimisation was attempted but attention was placed on source to load matching.

The main personalities at this institution are G.L. Katulka, M. Del Guerco, K.J. White, H.S. Burden and A. Zielinski. Refs [20][21][22][23][24] refer to this institutions work from the year 1991 to 1995.

The second group is in Fort Monmouth, NJ, and seems to focus mainly on solid-state switches (some initial research in 1989 into turn-off switches but focussing only on thyristors later) and then later on the integration of an ETC system on a

vehicle. The main personalities here are T. Podlesak, H. Singh and J. Carter. Papers [25][26][27][28] refer to this groups work.

2.9.2 Katulka *et al.* Year 1991 [20]

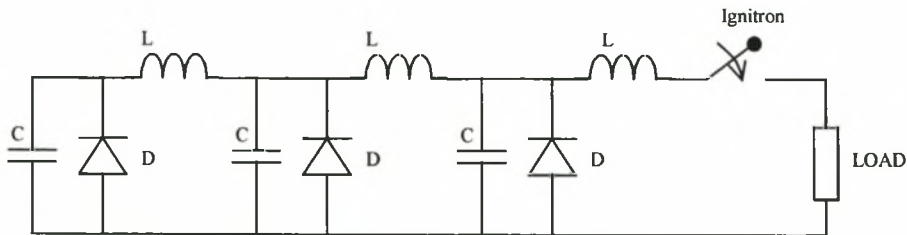


Fig. 2-10 Katulka *et al.* PFN [20]

Fig. 2-10 is a basic ladder network that depends on the values of the L and C parameters to determine the pulse form. Load matching is required which means that an accurate model of the load is required.

2.9.3 Katulka *et al.* Year 1992 [21]

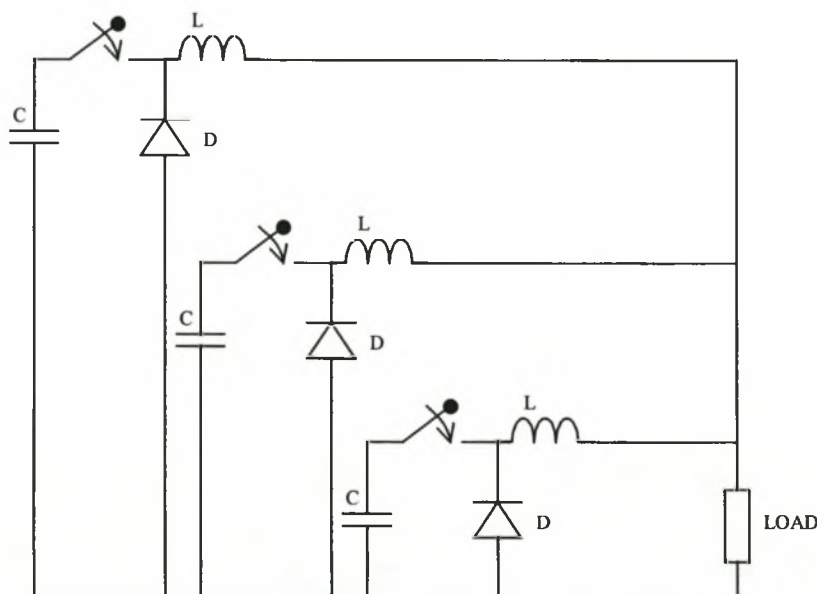


Fig. 2-11 Katulka *et al.* modified PFN [21]

This reference documents the circuit of Fig. 2-11 and is a technical report from the US army laboratory command. The topology has the advantage of allowing a great deal more control over the pulse shape. The constructed system is a simple 22 kJ energy system delivering a pulse of less than 1 ms, assumedly as an ETC ignition

pulse (this is not explicitly verified). An alternative to the above circuit was attempted when diode failure resulted. The switches (ignitrons in this installation) were moved to past the inductor and the diodes were in parallel with the storage capacitor. Currents of over 15 kA were achieved.

2.9.4 Katulka *et al.* Year 1994 [22]

Katulka *et al.* upgrades the circuit of Ref. [20]. An 8-module transmission line pulse forming network capable of delivering 300-400 kJ is constructed. The focus of the reference is particularly on the characteristics of the capillary itself. Research of this topology seems to have been taken over by M. Del Guercio at this juncture.

2.9.5 Katulka *et al.* Year 1995 [23][24]

Power diode failure continued to be a problem and Katulka *et al.* researched the reasons and provided potential solutions. Katulka focuses on the active pulse shaping of the topology of Ref. [21]. Experiments with a 100 kJ PFN were performed.

2.9.6 Podlesak *et al.* Year 1989 [25]

Podlesak *et al.* researched the application of GTO serialisation for a DC power supply. Explicit reference was made to the gating difficulties (high current requirements) of GTOs and the future of advanced devices (in particular the MCT) to these applications. Voltage sharing was performed using capacitors.

A 25 kV switch was to be constructed from discrete 4.5 kV 2 kA switches. This reference does not document the construction of this final switch.

Assuming that Podlesak was at this stage busy with ETC work, it can be assumed that this research was also aimed at inductive storage. The fact that Podlesak later researched turn-on switches (for capacitive storage) is noteworthy.

2.9.7 Podlesak *et al.* Year 1997 [26][27][28]

Refs [26][28] focus on research into high current SCRs. Commercially available devices are compared to a special 125mm thyristor. Current ratings from 25 kA to 110 kA of the 125 mm device are examined. The 125 mm device is specifically constructed to have a very low thermal resistance of 0.0033 K/W.

The advantage of capacitive storage devices with respect to silicon switches is that the I^2t rating can be utilised and the devices overdriven. Special packaging and

heatsinking of the 125 mm device indicates such specialised thermal management of silicon devices is a reality.

Table 2-7 Podlesak *et al.* capacitor based system data [27]

<i>Component</i>	<i>Size (m³)</i>	<i>Weight (kg)</i>
Capacitor PFN and switch	1.58	2700
Capacitor Charging inverter AC-DC	0.1	117
Generator	0.06	80
Total	1.74	2897
With 80 % stacking	2.18	
<i>With Battery Standby</i>		
Bi-directional inverter	0.2	174
Battery	0.36	843
Total	2.3	3914
With 80% stacking	2.87	

Table 2-8 Podlesak *et al.* Inductor based system data [27]

<i>Component</i>	<i>Size (m³)</i>	<i>Weight (kg)</i>
Inductors and switching	1.27	1120
Electro-chemical capacitors	0.36	240
AC-DC converter	0.45	160
Generator	0.075	100
Total	2.15	1620
With 80 % stacking	2.69	
<i>With Battery Standby</i>		
Battery	0.34	800
Total	2.49	2420
With 80% stacking	3.11	

The data of Table 2-7 and Table 2-8 is for a 4.3 MJ (load side) PFN with 3 “stored” shots [27]. Of distinct importance is that the suggested inductive storage is very different from that proposed by Soreq. It works in a different energy envelope,

uses electro-chemical capacitors as the IS and utilises superfluous system requirements. This is performed to effectively increase the IS voltage level to reduce charge time requirements and effectively reduce conduction losses of the turn-off switches. This is the marked difference if compared to Kanter *et al.* system, which also requires no silent watch as the silent watch capability is intrinsically provided for by the battery IS. However, the different energy envelope (between 1 and 10 MJ) may require alternative considerations not dealt with by Kanter *et al.* Thus this research is considered as an effective capacitor-based system comparisons but the inductor-storage research performed is considered as secondary to that performed by Kanter *et al.*

2.9.8 Summary

No documentation past January 1997 was found. The difference in opinion between the ARL and Soreq concerning capacitive and inductive storage needs to be considered. It is apparent that the ARL consider capacitive storage as the solution to high density PFNs, at least in the 1 – 10 MJ range.

2.10 Air Force Armament base, USA, and multi-MJ inductive storage

2.10.1 Introduction

In 1987, a large multi-MJ battery-based inductive storage project was initiated at Elgin Air force base, Florida, USA. The project was initiated as an improvement to the existing 10 MJ HPG-based system and 5 MJ capacitor based system. No volume or mass optimisations were under consideration. The system was composed of a very large battery bank (literally over 13,000 batteries), a fast charge inductor and an explosively operated turn off switch.

It appears that there are no central figures involved in the projects development. Refs [31][32][33][34][29][30] are used. Documentation is from 1987 and 1991 only.

2.10.2 Year 1987 [29][30]

These two references document the design and subsystem choice verification of the Elgin Air force base Battery supply shown in Fig. 2-12.

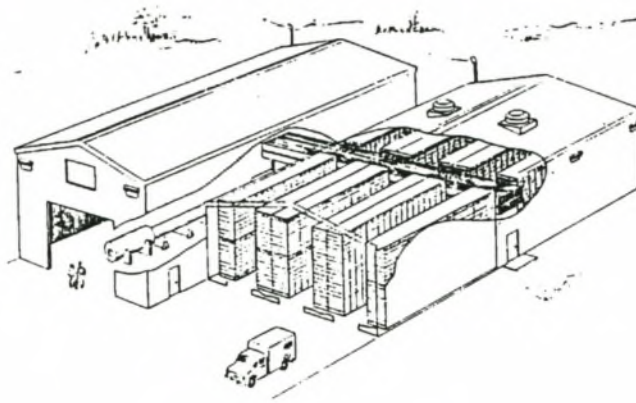


Fig. 2-12 Elgin Air Force base plan [30]

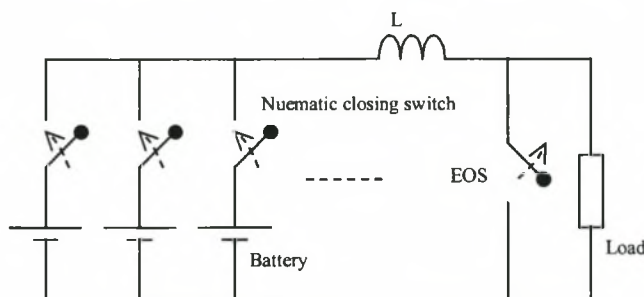


Fig. 2-13 Elgin Installation schematic [29]

The system is specifically for EM launchers and was rated at 200 MJ. The closing switches of Fig. 2-13 are make-break pneumatic DC contactors. The EOS is an explosively operated switch [33] and the storage element is a $68 \mu\text{H}$ 3 MA air-core inductor. A number of elements included in the references are not included in this circuit schematic (such as ESRs and stray inductances). Each battery branch or “gang” is composed of 24, 16-battery strings. There are 42 gangs. A great deal of attention was placed on the circuit parasitics and specific battery technology. The battery used was an automotive battery capable of delivering 2000 A short circuit current.

2.10.3 Year 1991 [31][32][33][34]

All four publications are from the IEEE Transactions on Magnetics vol. 27 1991. The references focus on the explosively operated switch, maintenance of the battery bank, battery failure rates and measurement systems. The explosively operated switch is a solid conductor switch explosively ruptured during commutation. A great deal of effort was performed in making sure that the circuit parasitics – the ESRs and stray

inductances – were correctly compensated for. Inductance of the load results in an energy reflection that needs to be absorbed by the switch.

2.10.4 Summary

Although this is an inductive storage system, it bares little relevance to the current project. The energy storage requirement and system volume makes the design method inapplicable to ETC applications. However, the careful focus on the parasitics is a consideration that needs to be mirrored.

2.11 Superconductors

2.11.1 Introduction

The advantages of superconductor technology are obvious. No thermal loss means that current can be stored indefinitely. If superconducting switches are a viable option, no conduction losses (a major problem) need to be dealt with. However, the cryogenic requirements, material properties problems and immaturity of the field poses a number of challenges.

Some consideration has been given to the application of superconductors to the field. Some research was performed in 1991 in America [35] on the feasibility of a high temperature superconductor (HTSC) coil for EML technology. The focus on the research is specifically on the material properties of the conductor at high temperatures (20 K). Some work was performed in France in 1996. Magnet Motor, Germany, have been busy researching various superconducting inductive storage topologies and came out with a product in September 1999.

2.11.2 Year 1991 [35]

The prime concerns dealt with in this paper were the material properties of the superconducting material. The problem behind SMES (super conducting magnetic energy storage) technology or large-conductor superconductor applications is in the manufacture of bulk conductors; various material property problems arose. These – and possible solutions – are mentioned.

Consideration of HTSC with respect to EML requirements are taken into account. In particular, reference is made to hyper-conductors and the possibility of

superconducting switches. The paper considers liquid hydrogen at 21K to be the ideal HTSC coolant.

2.11.3 Year 1996 [36]

Superconductors have the material property problems of having a limited current density and operational temperature. The storage of high currents in such a coil is difficult. However, Ref. [36] proposes a method using a transformer based superconducting PFN to store and commutate energy. The system is composed of a superconducting primary (cooled with liquid helium) and a coupled copper secondary. Commutation is performed by quenching the primary (specifics are not given). Upon quenching, the whole primary is brought out of super-conductivity and energy is transferred to the copper secondary. There is no primary commutation switch so the full reflected load voltage is apparently distributed across the whole primary.

The paper describes the full electrical design of such a configuration. The advantages of such a system are obvious; indefinite storage of the energy before commutation, load matching with the transformer action and no excessive voltage stresses are placed on the opening switches (there are none – the primary is a short circuit). However, very little practical detail (in particular fabrication of the full system, quenching methods, heat exchange) is given.

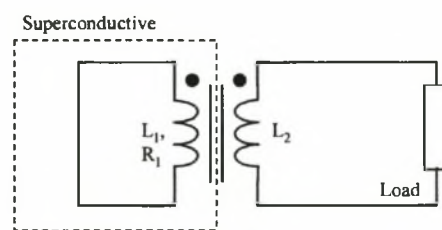


Fig. 2-14 Superconductor transformer-based PFN

2.11.4 Years 1997, 1999 [37][38]

Magnet Motor published a paper discussing their work on a modular superconducting inductive storage element for 4 MJ EML applications shown in Fig. 2-15.

In 1999, a 6-module product was brought out (with slight modifications) with energy storage of 500kJ. The system is intended to be installed on a mobile vehicle. S_B is the bus switch (zero current closing and non-commutation opening). CS is a closing switch. OS is the turn off commutation switch.

Three stages are required, the charge, storage and discharge. During the charge stage, S_B is closed, CS is open and OS is closed. During the storage stage, S_B is open, CS is closed and OS is closed. The IS is thus removed from the circuit. For the discharge phase CS is kept closed (but is not conducting) and OS opens and results in the energy transfer to the load through the de-coupling diodes. This is a similar circuit (modified XRAM) to that used in this research.

Both CS and OS are superconducting switches.

The superconductor is NbTi in a Cu matrix. The 1997 reference discusses the design procedures required to specify full system construction. The 1999 reference documents some system results. The focus of the two shifted from EML technology to ETC technology. Where not stated, all further references are to the 1999 product.

S_B is not specified but has no extreme operating conditions. CS is also not specified but must be superconducting (the storage stage requires zero dissipation).

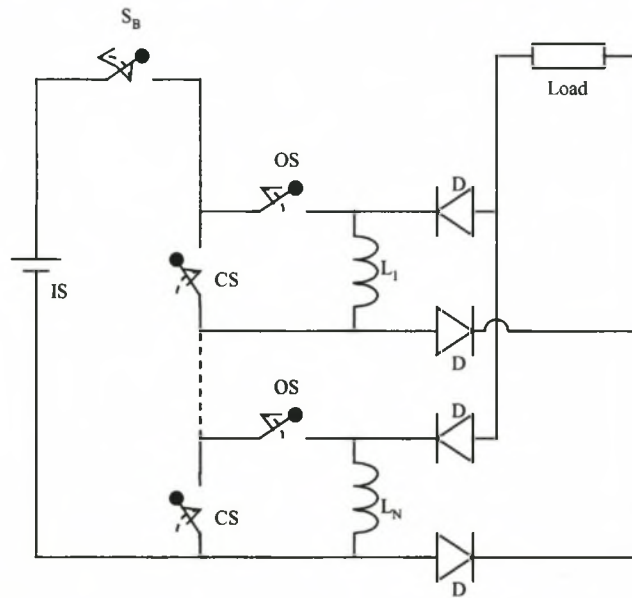


Fig. 2-15 Magnet Motor superconductor topology [38]

It need not be a fast or voltage protected switch ([37] considers a thermally triggered switch to be sufficient). The OS is the challenging switch and is composed of a superconductor rated at 2 kA. Triggering is performed via a (assumedly externally) current pulse to drive the superconductor into normal conduction (60 Ω). The cryogen is a helium bath.

It appears (the reference is not clear) that the priming maximum is 1.6 kA and the load maximum is 9,6 kA. The full volume assuming less the refrigeration peripherals is 400 l.

The IS is composed of a Magnet-Motor Flywheel with a chopper stage intermediate connection.

2.11.5 Summary

It appears that a number of the challenges of superconductor technology as applied to ETC PFNs have been met. In particular, the reduced (zero) thermal loss in the inductor and switch are obvious and important advantages. It can be assumed that as there is no field relaxation into a superconductor, none of the losses as discussed by Kanter *et al.* occur.

However, not sufficiently dealt with (at least not the publications) is the extra refrigeration costs and safety issues as concerns liquid helium aboard a AECV.

Of importance too is the current levels used in Ref. [38] which requires a priming current of 1.6 kA. At this current, a high inductance storage device is required. For 500 kJ (as quoted) this results in a total coupled inductance of 0.36 H; for a 6-module ideally coupled device this results in a 11 mH / per unit self inductance (which results in an 11 mH apparent inductance during a parallel discharge – as specified). According to calculations discussed by Kanter *et al.* and adopted in this project, these values are too high and do not allow for sufficient coupling to the load, typically modelled as a 100 mΩ resistor; it is possible that an additional transformer stage is also included into the system (this assumption is not verified). Ref. [38] does show some practical results. The solution to this dilemma is not further researched.

However, if a non-superconductor system was to be developed with these ratings, it seems that the specified volume values could be sufficiently matched using semiconductor switches and commercially available technology. The six switches are rated at 1.6 kA, 4 kV.

2.12 Capacitive technologies

2.12.1 Introduction

Capacitor-based PFN systems have a number of advantages over its static counterparts. Most importantly, the commutation hardware required for capacitor-based systems is a turn-on switch only.

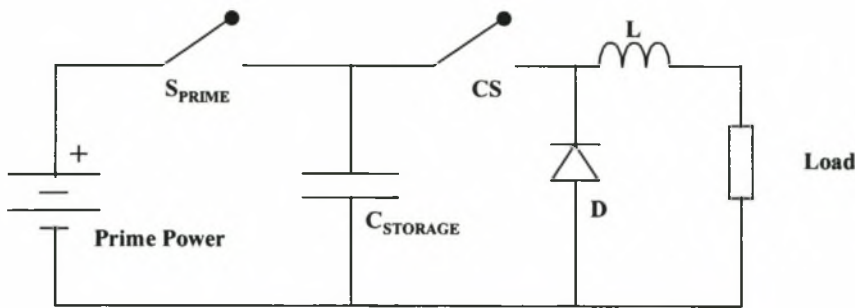


Fig. 2-16 Generic capacitor-based system

Most millisecond capacitor based systems have Fig. 2-16 as its primary building block. The storage capacitor $C_{STORAGE}$ is charged by the Prime Power source. The charging speed is application and technology specific. When fully charged, the Prime Power source is decoupled (usually). The closing switch CS closes and energy is transferred to the load. Here two different systems are possible; either the capacitor is discharge directly into the load and the inductor L is very small and the load and the storage capacitor determine the discharge pattern or the inductor L is used as a pulse former and freewheels when fully charged.

The first method can be used if a modular capacitor based system is used (and active pulse forming is implemented) or if the load itself is inductive and the desirable pulse form is achieved without the added inductor. However, this is generally not the case.

The capacitor discharges resonantly into the inductor. At this stage the load can be ignored. Upon full discharge (where the capacitor voltage has reached zero and the load current is now maximum), the inductor continues to force the current to flow forcing commutation through the diode D . Pulse forming is performed further with the inductor – load discharge pattern.

Of interest are the following points:

1. The switch itself need only conduct during the discharge of the capacitor. Sometimes the switch is placed after the diode branch and as a result the switch must conduct the full load current throughout the load discharge.
2. A reverse voltage occurs across the capacitor; this generally needs to be avoided.
3. Transfer of energy from the source (capacitor) to the load (inductor and load combination) occurs naturally as a part of the resonant cycle. No force commutation is required.
4. A component of the stored energy is not transferred to the load and remains in the capacitor.
5. The capacitor based system is in most cases similar to the inductive storage PFN, with the difference that the IS is composed of capacitors and self-commutates.

2.12.2 Capacitive PFNs world wide.

In 1995, a number of papers were published in the IEEE Transaction on Magnetics.

A 500 kJ installation was documented in DRA, England. The system was composed of 10 Maxwell 50 kJ units [39].

A 2.4 MJ system composed of 8 Maxwell 300 kJ units was installed by the British Aerospace Defence to research ETC technologies [40].

A 52 MJ system composed of sixteen 3.25 MJ modules at the US Army Research, Development and Engineering Centre is documented [41]. Of interest here is the use of “resistance balancing” and a RAG, or rotating air gap, switch.

In January 1997, PI brought out a compact 250 kJ system with overall PFN energy density of 1.2 MJ/m^3 fired with a vacuum switch and using a fully shielded inductor [49].

E. Spahn and G. Buderer at the French-German Research institute of Saint Louis researched a 50 kJ PFN between 1995 and 1998 [42][43][44][45]. The main focus of the research was on the closing switch (a SCR) with high current ratings.

2.12.3 Capacitor Technology

The only reason non-capacitive systems would be considered for volume-optimised ETC sources is that the capacitor itself does not have sufficient power and energy density levels. Due to this shortcoming, a great deal of research has been performed on capacitor technology. In general, the discharge rate required in electric guns means that high density electrochemical capacitors are not applicable. As a result, in general

robust AC capacitors need to be utilised. Energy densities of less than 1 MJ/m^3 may be achievable but for pulse applications, the transferable energy falls to less than 70 %.

An option, as discussed in Ref. [27], is to replace the battery with electrochemical capacitors (which have a greater power density but lower energy density). Another option is to use new pseudo-capacitance – or supercapacitor – technology tabulated in Table 2-9. These capacitors generally have very high storage contents – values of many Farad are speculated at – but the disadvantage of low operating voltage and low transfer efficiency and di/dt's. The use of specialised capacitors has the disadvantage that although capable of storing the correct amount of energy, transfer of this energy in the required time frame is not possible and transfer efficiencies of 50% result. As a result it may be better to depend on older technologies with a higher efficiency.

Table 2-9 Some supercapacitor data [46]

<i>Name</i>	<i>Electrode Electrolyte</i>	<i>[kJ / kg]</i>	<i>V [V]</i>	<i>Cap [F]</i>
NEC Supercapacitor NY	Carbon / sulphuric acid	1.2	5	2.2
Panasonic	Carbon / organic	7.9	3	500-1500
Pinnacle Research	Mixed oxides / sulphuric acid	18	100	0.01
Maxwell / Auburn	Carbon-metal / KOH or organic	6.8 or 25	1 or 3	55 or 13

In 1996 a trans-national perspective (of the USA) was performed [47]. Predictions as to the relevant technologies were made and the important points tabulated in Table 2-10.

Table 2-10 Capacitor technologies for capacitor IS [47]

<i>Capacitor system</i>	<i>[kJ / kg] Now (1996) / Future (2010)</i>
Polymer film	0.4 / 20
Electrolytic	0.2 / 2

Ref. [48] discusses the bases for third generation capacitor technology applicable to capacitor PFNs. Of particular interest is again the Physics International capacitor-based PFN with full system volume density of 1.2 MJ / m^3 [49].

Table 2-11 Capacitor technology generations [48]

<i>Generation</i>	<i>Technology</i>	<i>Energy Density kJ / m³</i>	<i>Density kJ / kg</i>
1	Paper / Castor oil. Al. Foil	550	0.3
2	Metallised Polypropylene	800	0.64
3 (current)	Based on : Polymer Film Metallisation Impregnation	2000	

The capacitor is a metallised electrode PVDF electrolyte unit (with 2.5 MJ / m³ density and up to 70% efficiency). Arguments are given as to why this technology should be used over the older 2 generation polypropylene based capacitors.

2.12.4 Summary

The advantages of capacitive based technologies over other static systems have been described. In particular, little thermal loss during the charge phase and the relative simplicity of the closing switch (and its operation) are distinct advantages. The low energy density of capacitors and the required capacitor charge phase (in some cases a problem if no robust prime power is available or if the silent watch specification needs to be met) are the disadvantages. In particular, the low energy density means that large – energy systems are very bulky and not suitable for many applications.

However, if high-energy density capacitor-based systems are a viable option, the design and working of such a system would make it the better option.

2.13 Opening switches

2.13.1 Introduction

Inductive storage systems require robust circuit elements. For a single module system, the IS needs to be able to deliver the full load current. The discharge of an inductive supply into an inductive load by definition results in very high voltage peaks.

Most challenging however is the opening switch requirements. The switch must conduct the full priming current for the charge cycle (for long charge systems which generally characterise volume optimised systems this could reach into the half – second time duration). As a result, conduction losses must be minimised. At

commutation, the opening switch must force commutate the current from the priming source into the load. The switch, in its off state, must hold off the full load voltage and not re-close or fail.

Many different opening switches and mixed-switch topologies have been suggested and used. For high current applications, mostly commutation assisted mechanical switches are used. This section highlights the applicable turn-off switch technologies to inductor-based systems and the switches considered for this project.

2.13.2 Semiconductor only turn-off switches

The relevant switches include Gate turn-off thyristors (GTOs), Insulated gate bipolar transistors (IGBTs) and gate commutated thyristors. The main switch-device types are displayed in Fig. 2-17. Traditionally, GTOs have cornered the market due to the switches high ratings; devices of 6 kV 6 kA ratings are available. The GTO is based on the thyristor and as a result has low on-state losses.

The disadvantage of using GTOs are firstly the comparatively slow switching times of the devices and the current based driver that is required. Typically, GTOs require more than 20% of the its anode current to turn off. As a result, the commutation hardware is often more voluminous than the switch itself. Also, the GTO cannot typically be overdriven and large turn-off snubbers are generally required.

In general, MOSFETs and other majority carrier devices are not applicable to high-power applications as their conduction losses at high currents are excessive.

IGBTs implement a MOSFET-controlled bipolar transistor. As a result the gating advantages of the MOSFET (voltage controlled low power gating) are coupled with the conduction advantages allowed by the bipolar structure. The silicon structure of the devices is relatively complex and low thermal resistance structures are not possible or very difficult to manufacture (such as hockey-puck devices).

As a result, the current carrying capabilities of IGBTs are lower than its counterparts, and where necessary die-paralleling is implemented. For NPT devices (non-punch through – the majority of IGBTs), the device is mostly MOSFET-based and a positive temperature co-efficient means paralleling is simple. This is a distinct advantage over the minority-carrier devices such as GTOs, SCRs (or thyristors), BJTs and diodes.

IGCTs, or GCTs, are a new device on the market and are superior to all the other devices in that the gating advantages of the MOSFET (voltage controlled low power gating) is combined with the superior conduction of the SCR. A product with 4.5 kV 4 kA is reputedly available from Mitsubishi [51]. However, past experience with similar devices such as the MCT (MOSFET controlled thyristors) and MAGT (MOSFET assisted gate-triggered thyristor [50]) where the device did not reach market expectations teaches that caution is required in depending on untested technologies. However, it appears that if GCTs prove to be reliable then implementation of these devices over its counterparts should not prove too difficult.

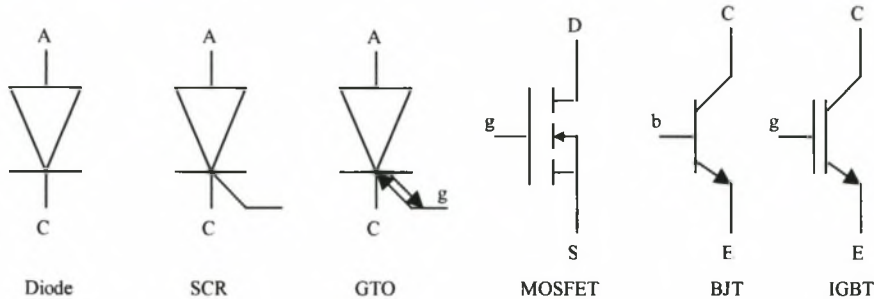


Fig. 2-17 Silicon switches

2.13.3 Device serialisation and paralleling

Serialisation and paralleling of silicon devices is necessary if a high power switch is to be constructed.

A high-current matrix GCT based switch has reportedly been produced [52]. This is work performed under TNO in the Netherlands. To date a 50 kA module has been developed. Current sharing of the devices is done using both matched devices and unmatched devices. Apparently, the devices shared sufficiently well. No voltage serialisation was performed. This research is particularly worth keeping an eye on.

Device serialisation is in general a distinct problem. Due to manufacturing processes, devices do not switch in exactly the same manner. As a result, during a switching transient the voltage across one device in a series string may be higher than its counterparts. Some sort of enforced sharing is necessary. This is fully researched in section 3.11.

2.13.4 Resonant commutation of closing switches

An SCR is a very robust device. It has the advantage of being able to block very high voltages and conduct very large currents. The device is however only a turn-on device. The device is commutated off when the voltage drop across it is reversed.

Some converter applications use force commutated devices where some resonant circuit enforces a reverse (or zero) voltage across the thyristor. Research into the force commutation of a thyristor is incorporated into the scope of this project and is documented in Ref. [53] and the basic switch idea is shown in Fig. 2-18.

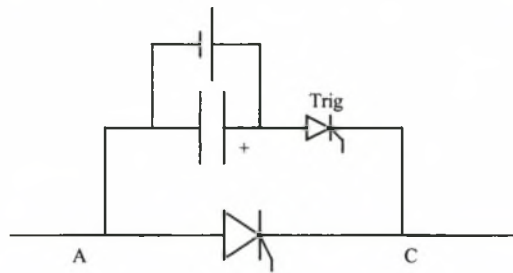


Fig. 2-18 Force commutated thyristor

When the switch needs to turn off, the switch *trig* is initialised and the capacitor effectively discharges into the main switch. This is necessary as a capacity of charge within the thyristor needs to be either recombined or drawn out of the device to ensure that the SCR does not switch on again when a forward voltage is again re-applied. This is documented in the device datasheets as a charge Q_R or a time t_Q . This time is a duration for which the device must be reverse biased to ensure that re-firing does not occur.

The problem with this topology is that for high current devices this time is very large (longer than a millisecond in some cases) and as a result the capacitor has to be of a very large value of higher than 100mF. This is not desirable as the capacitance volume would be correspondingly high. Also, unless the switch *trig* is switched of the capacitor follows the load voltage and as a result cannot be polarised. By turning 'trig' off this can be avoided. For high-power implementation, some sort of resonant discharge will have to be incorporated into the circuit as well; however, in depth research into this facet was not performed.

Implementation of the above circuit using a spark gap in place of the SCR has been performed in the course of this project by an undergraduate student at PEG.

When on, a plasma column conducts between two electrodes. When commutation occurs, the capacitor effectively absorbs the spark gap energy forcing the spark gap voltage to zero (and below) and allows the air column between the two electrodes to re-establish itself. The current is switched out of the opening switch and into the load and the spark gap voltage rises (assuming no re-firing of the spark takes place). Upon commutation this voltage is brought down to zero. Energy is commutated from the source to the load as depicted.

Favourable results were achieved at low power levels but the research was not taken further. It is observed that the spark-gap technology is very involved; further research into this technique would require more time, money and manpower than what was available. Also, thermal considerations with the switch seemed to make a long charge – 300 ms – system non-viable.

In 1995 and again in 1999, Delft University published a topology similar to that above [54][55]. The circuit was however focused on the assisted zero-current commutation of a mechanical switch.

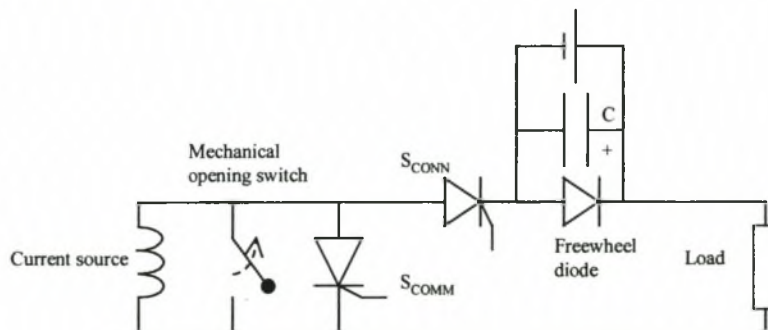


Fig. 2-19 Delft zero-current opening switch [54][55]

This circuit of Fig. 2-19 is different from those mentioned before as it considers the current source to be constant and allows for multiple switching.

Interval 1: The opening switch is closed (conducting), the connecting thyristor (S_{CONN}) is off and the commutation thyristor (S_{COMM}) is off. This is the storage stage.

Interval 2: S_{CONN} is switched on. The current increases through the capacitor C and decreases through the opening switch. Resonance of the capacitor C , the load and the opening switch determine the relevant times.

Interval 3: The opening switch is opened at zero current.

Interval 4: The capacitor C is fully discharged and the current source freewheels through the freewheel diode. The capacitors voltage is clamped at zero.

Interval 5: The commutation thyristor is closed. Current decreases through the load and increases S_{COMM} . The opening switch is then closed.

For one-shot use (where the source inductor current falls to zero) S_{COMM} is not necessary. This topology has the advantage that the capacitor bank (the largest volume component) can be of a high energy density polarised technology.

2.14 Summary

Research documented mainly in IEEE publications is considered. The two main schools of thought is inductive storage (in the <1 MJ range) represented mainly by Soreq in Israel and capacitive storage, represented in Europe and America but particularly by institutions concerned with the US military. Alternatives – such as inertial storage – are also considered in certain parts of the world.

This chapter compromises the full background study performed. The term PFN encompasses a wide field, with widely different topologies required for the varied applications.

This project is specifically concerned with millisecond pulse PFNs using inductive storage techniques.

Of the inductor technologies applicable, a 4-stage direct-drive modular inductor of the Brooks [73] dimension and the XRAM topology [6] is chosen. This allows for a volume-optimised inductor [73] and pulse shaping on the load side. The IS is chosen as battery storage. The switches are solid state switches.

Volume concerns and electrical concerns are considered in more detail in the following chapters.

CHAPTER 3

CIRCUIT ANALYSIS OF THE XRAM TOPOLOGY

3.1 Introduction

This chapter introduces both the standard and modified XRAM topologies and discusses the topology and resultant operational differences. Analyses of all the transients that occur during the full charge and discharge process of the modified XRAM topology are presented.

Of importance are the device voltage levels that occur, the nature of the steady-state discharge transients and their effects and also the effect of the system parasitics on each transient. Where required – and where possible – mathematical models of certain phenomena are developed to aid in the development of generalised results for these phenomena.

Section 3.3 shows that 4 modules are considered optimal for a volume-optimised system. Inherent in the design of a modular volume optimised system is the requirement for the storage stages to be balanced (verified in section 3.3). This means that the module self-inductances must be equal and that the coupling between each module must be homogenous (equal). This is assumed throughout the following analyses. As it is probable that slight inductance value variations will occur; the relevant specific cases are also analysed.

3.2 XRAM topology

3.2.1 Standard XRAM topology

The term XRAM is the inverse of the term MARX. A MARX generator is used to generate a high voltage through the parallel charging of devices (capacitors) and the series discharge of these devices. MARX technology is associated with low-energy, short time-span (nanosecond to microsecond) pulse generation.

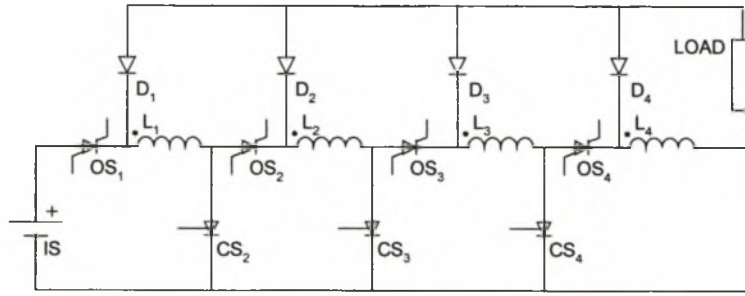


Fig. 3-1 Standard 4-module XRAM topology

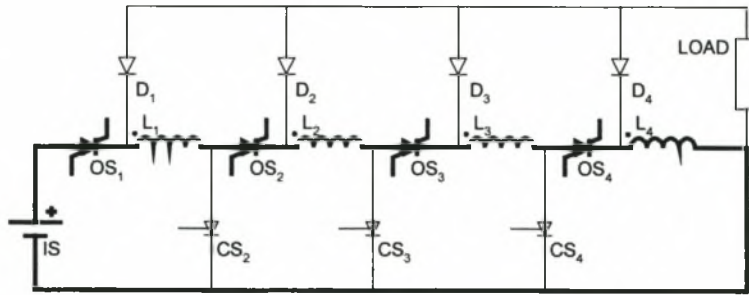


Fig. 3-2 Charge cycle of standard XRAM topology

The XRAM generator is typically associated with high-energy ms pulse requirements and utilises serial charging and parallel discharging of storage devices, typically inductors. The most obvious advantages of modularity in an inductive supply are that it allows for a lower I_S current requirement and for active pulse shaping on the load side.

Fig. 3-1 shows the most commonly applied XRAM topology [6]. Each module consists of a storage element L_x , opening switch OS_x , closing switch CS_x and rectifier D_x where $1 \leq x \leq n$ and n is the total module number. CS_1 is not required. Module inductive coupling as shown in Fig. 3-1 is not required for circuit operation, but is advantageous in increasing the inductor energy density.

The charge cycle as shown in Fig. 3-2 is initiated by the closure of all the OS s. The charge cycle follows an L/R time constant determined by the inductance of the supply and the ESRs of the charge path. The diodes protect the load from a current pre-initialisation. The discharge paths of the full parallel discharge configuration are shown in Fig. 3-3. A single module switching action is performed through the closing (turn on) of the module CS followed by the opening (turn off) of the OS . Timing considerations between these two devices need to be taken into account, depending on

the switch technology. The module diode D becomes forward biased and the module inductor effectively free-wheels through the load.

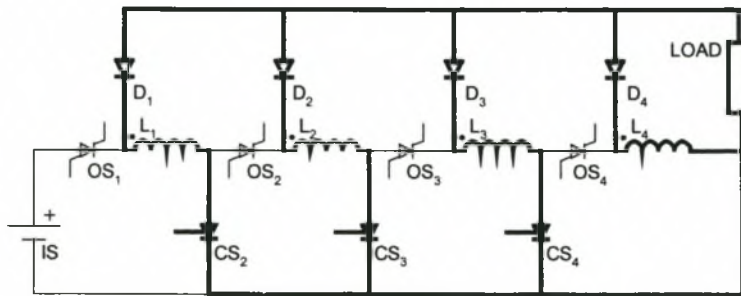


Fig. 3-3 Discharge cycle of standard XRAM topology

Different module switching sequences are possible. It is in the designers interest to de-couple the IS from the discharge paths during discharge, module 1 is generally switched first. This initiates the energy transfer to the load through the forward biasing of D_1 and isolates the IS from the back-end. The remaining modules are switched after time delays determined by the designer.

The switching sequence assumed in this project is 1 3 2 4, where modules 2 and 4 are switched together. This allows for a balanced energy transfer between all the modules and the load (for coupled or uncoupled inductors).

3.2.2 Modified XRAM topology

Fig. 3-4 shows the modified XRAM topology, developed in the course of this project. It differs from that described in Fig. 3-1 as it has no closing switches and requires different charge return paths and discharge free-wheel paths. This topology has the following advantages:

1. No CSs are required. This results in reduced system cost and volume.
2. Module commutation is determined solely by the opening switch; no compatibility problems between switch times of the CS and OS occur.

The only disadvantage of this system is that a small voltage occurs across the load during the system charge cycle; this is described in the following section. This voltage is always less than the IS voltage and varies slightly during the charge cycle. For volume optimised systems the IS voltage is more than an order lower than the expected load voltage during discharge.

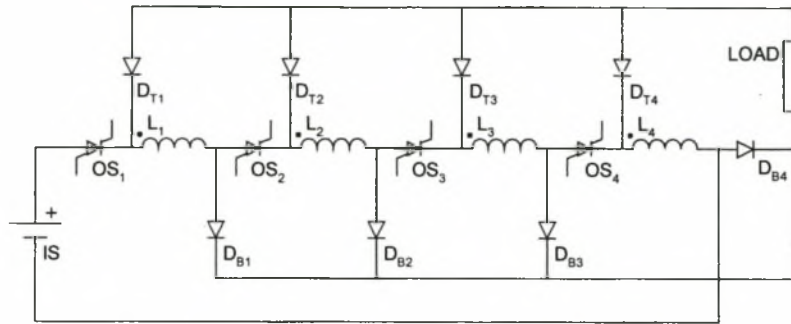


Fig. 3-4 Modified XRAM topology

For short-circuit loads such as the ETC load some form of load protection must be incorporated (such as a small spark gap within the load capillary). This is the responsibility of the capillary-load designer, however. If a switch or solid-state device external to the capillary is used for voltage hold-off during the charge cycle, it will need to conduct the full load current during the whole discharge cycle. This will require additional hardware and result in a full hardware requirement equal to that of the standard XRAM topology and as a result the topology requirements become effectively identical. Thus it is clear that only load protection within the capillary validates the use of the alternative XRAM topology. For loads where such protection is impossible – such as an EM load – the standard topology needs to be used.

The topology is analysed in the following sections. Each switching stage is considered individually.

3.3 Volume and waves hape dependence on modularity

This section is included at this early stage as module number and balanced discharge considerations play a large role in both the circuit analysis of the XRAM topology and the system volume optimisation process. Formal proofs of system dependence on modularity are given in section 5.2. Integral to this proof is the equation

$$L_{ST} = R_L t_d n^2, \quad 3-1$$

which is proven in 4.5 but repeated at this stage for the sake of clarity. L_{ST} is the total required inductance, R_L the load approximation, t_d the minimum allowable discharge time and n is the module number. The derivation of Eq. 3-1 requires all the module inductors to be balanced. Without such a balanced system, the volume relations discussed in section 5.2 are no longer applicable and the IS and inductor volume is no longer independent of module number.

The level of modularity required is now discussed. Eq. 3-1 is applicable to coupled and uncoupled systems. However, use of the Brooks coil to incorporate the full inductor value results in an inductor volume optimum. As a result, inter-inductor coupling is required to allow for a system volume minimum. Analyses in section 3.7 and Appendix A show that slight inductor imbalance during a discharge state results in degradation of the current in the inductors during discharge; that is, the currents diverge where the ideal would be that they remain the same.

For large module inductor value differences as discussed in section 3.7, this degradation occurs rapidly (in the order of a few tens of micro-seconds) and it is clear that it is not of use to allow such unbalanced inductor discharge if the desired wave shape is to be retained. Inter-module coupling worsens this effect appreciably. As a result of this, the only useful, or stable, discharge states occur when the branch inductors are balanced. This also means that each useful switch state is not equal to the number of modules. For instance, a 4-module system has 3 balanced switch states. With reference to section 3.7 (Fig. 3-5), these occur when Q_1 is switched, Q_3 is switched and when Q_2 and Q_4 are simultaneously switched. The next viable module number is 8 (6 also allows for only 3 states). For an 8-module system there are four useful switch states.

The equation

$$n = 2^{\text{states}-1}, \quad 3-2$$

describes this relation formally. Other module number combinations are possible, but result in fewer stable discharge states.

Although 8 modules are theoretically possible, an 8-module system would require excessive – and volume-consuming – construction considerations. Four modules are thus considered the optimum.

3.4 Charge cycle

Foreword

Use of the modified XRAM topology will result in a voltage across the load during the charge cycle. An actual ETC load cannot allow current to flow in the load during the charge phase and some sort of load protection will need to be incorporated. However, in the prototype this current will flow and it is thus in the designers interest to analyse the phenomenon sufficiently. A complete analytical solution of the system

equations during the charge phase is cumbersome; no generalised results can be drawn from this. Assumptions are made that allow the development of simpler equations that give an indication of the coupling between the system parameters and allow for the development of generalised results.

It is observed that if current is allowed to flow in the load, and diode D_{B1} conducts, then a negative voltage is induced by L_1 on L_2 for non-zero coupling. This results in one of two scenarios: either this negative voltage falls across Q_2 , which is on at this time. For some switch technologies, this must be avoided. If the switch is equipped with an anti-parallel diode (as is the case in the prototype) then this diode forward biases and current flows effectively backward through the switch module. It must be made clear, though, that for a protected load, the current through L_1 equals that through L_2 , and no reverse voltage will result.

Equivalent charge paths

All the calculations and discussions are based on the assumption that the system is balanced. Fig. 3-5(b) shows the relevant voltage and current referencing.

At time $t = 0$

At the start of the charge cycle, the current is zero. IGBTs $Q_1...Q_4$ are conducting and $v_{CE} = 0$ for all the devices. Not included in the circuit are the anti-parallel diodes across the IGBTs. The voltage $v_{LOAD} = 0$. Examination of Fig. 3-5(a) shows that an initial voltage condition can be derived. If L_2 was to experience a positive voltage (as would be expected), then the voltage loop $L_2 - D_{B1} - LOAD - D_{T3} - L_2$ would result in the forward biasing of diodes D_{B1} and D_{T3} . Likewise for L_3 and diodes D_{B2} and D_{T4} . As no current is flowing at this time, v_{L2} and v_{L3} are clamped to zero volt. With $L_1 = L_4$ and homogenous coupling, the inductors L_1 and L_4 equally share the full IS voltage. Furthermore, the voltage loop $L_2 - D_{T3} - D_{T2} - L_2$ (assuming D_{T3} is forward biased, but not necessarily conducting, and $v_{L2} = 0$) shows that the diode D_{T2} (and by the same procedure D_{T4} and D_{B3}) is also clamped at zero volts. As a result of this, the diodes D_{T1} and D_{B4} (with the help of voltage loops $L_4 - D_{B4} - LOAD - D_{T4} - L_4$ and $L_1 - D_{B1} - LOAD - D_{T1} - L_1$) are reverse biased with a voltage equal to half the IS voltage.

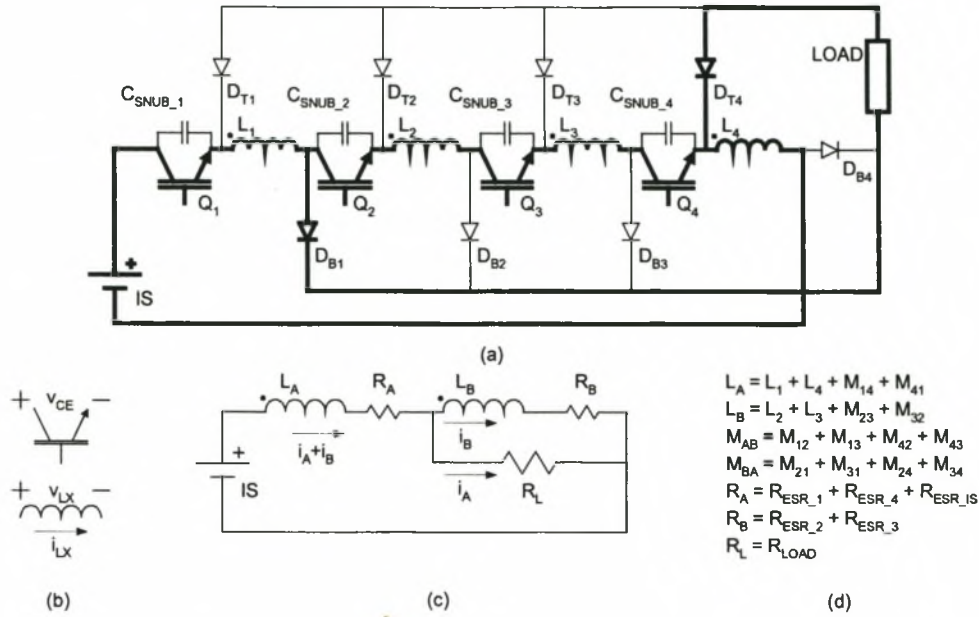


Fig. 3-5 Charge cycle and equivalent

At time $t = 0^+$ and $t > 0$

The available current loops are set in bold in Fig. 3-5(a). The main charge path $IS - L_1 - L_2 - L_3 - L_4 - IS$ is clear. It is also clear that current must flow through L_1 . This being the case, then the mutual coupling M_{12} could result in V_{L2} being non-zero and positive. If Q_2 is capable of holding a reverse voltage during its on state, then no reverse current will flow. However, the diode D_{B1} is still forced to remain forward biased and current will still flow to the load during the charge cycle. The constructed prototype does allow for a reverse current to flow through the Q_2 anti-parallel diode. This both forces the diode D_{B1} to conduct and for diodes D_{B2} and D_{B3} to become reverse biased. Even for zero coupling, L_2 is parallel to the load and D_{B1} will conduct. Diode D_{T2} is at this stage effectively parallel to the load and accordingly reverse biased. Current is also flowing through L_3 at this stage and v_{L3} is also non-zero and positive. If diode D_{T3} were conducting, then diode D_{T4} would clamp v_{L3} to zero; this is not possible and as a result D_{T3} is reverse biased. The only non-contradictory current flow paths are thus evident. These paths remain conducting through the duration of the charge cycle. Fig. 3-5(c) is a simplified system schematic showing only the conducting paths. Fig. 3-5(d) gives the relevant quantities and their relation to Fig. 3-5(a).

Charge cycle initial transient

It is observed in the following section that the initial transient and steady-state load current during the charge cycle is of an order of magnitude less than the charge current for the prototype and could be considered negligible. However, the initial transient results in a negative current flowing through an on switch. Such a phenomenon may influence the affected device and is thus of interest to the designer. It is formally modelled in the following section.

Coupled time constants

The current and device referencing of Fig. 3-5(c) are slightly ambiguous; this is performed to ease the calculation process. For a front-end matched system, $IS_{ESR} = L_{ESR_TOT}$ (refer to section 4.3) which for Fig. 3-5(c) and (d) translates to $IS_{ESR} = 4R_{ESR_X}$ where R_{ESR_X} refers to a module ESR. In order to generalise these results, it is assumed that $R_A = R_B = R$. In both cases, these ESRs are of the same order and it is only the tendency, in particular, that is of interest. In addition, this substantially simplifies the circuit equations and provides an indication of the coupling between the load resistor and the device ESRs and enables the designer to model the effects separately. The results will not necessarily be accurate in providing current or voltage magnitudes, but these considerations are discussed where relevant. For a balanced system, $L_A = L_B = L$ and $M_{AB} = M_{BA} = M$ are assumed.

The equations

$$IS_V = L \frac{di_A}{dt} + (L + M) \frac{di_B}{dt} + (R + R_L)i_A + Ri_B, \quad 3-3$$

and

$$(L + M) \frac{di_B}{dt} + M \frac{di_A}{dt} + Ri_B = R_L i_A, \quad 3-4$$

are derived from Fig. 3-5(c). The resultant equations (using maple) are

$$i_A = \frac{IS_V}{R + 2R_L} \cdot \left(1 - e^{\frac{R + 2R_L}{L - M}t} \right), \quad 3-5$$

and

$$i_B = \frac{IS_V}{2R} e^{-\frac{R}{L + M}t} + \frac{IS_V}{2(R + 2R_L)} e^{-\frac{R + 2R_L}{L - M}t} + \frac{R_L IS_V}{2R(R + 2R_L)}. \quad 3-6$$

Of interest here is the form of the two time constants. It is observed that for the systems of interest here (including the 500 kJ system and the prototype) $R_L > R$ (by at least an order). It appears therefore, by analysis of the time constants, that the coupling is relatively weak and that it is possible to separate the two system time constants and assume they are independent.

Uncoupled time constants

Matters can be simplified by defining uncoupled circuits; one dependent on the load resistance alone, the other on the ESRs. Both are of interest. Firstly, for the R_L circuit, it is assumed that $R = 0$. By recalculating Eqs 3-3 and 3-4 with $R = 0$, the solutions

$$i_{load} = i_A = \frac{IS_V}{2R_L} \left(1 - e^{-\frac{t}{\tau}} \right), \quad 3-7$$

$$i_B = \frac{IS_V}{4R_L} \left(e^{-\frac{t}{\tau}} - 1 \right) + \frac{IS_V}{2(L+M)} t, \quad 3-8$$

and

$$IS_I = i_B + i_A = \frac{IS_V}{4R_L} \left(1 - e^{-\frac{t}{\tau}} \right) + \frac{IS_V}{2(L+M)} t, \quad 3-9$$

where

$$\tau = \frac{L-M}{2R_L}, \quad 3-10$$

are calculated. The effect is comparatively fast. It is observed using a numerical simulation package and the full circuit model that the effect of the device ESRs on this phenomenon is negligible (less than 1% for typical system parameters) and that for the initial few milliseconds (before the effect falls away), Eqs 3-7 to 3-10 can be used to approximate the system current magnitudes accurately.

Fig. 3-6 displays measured and calculated results from Eqs 3-7 to 3-10. i_{L1} is equal to IS_I and $i_{L2} = i_B$. It is observed that the uncoupled transient model is in good agreement with measured results. The system values used are $R_L = 2.6 \Omega$ (from correlation with the actual system values of the prototype of section 6.7.4), $L = 8 \text{ mH}$, $k_c = 0.96$ and $IS_V = 108 \text{ V}$. It is observed that the load current stabilises very quickly. This current remains relatively constant throughout the charge cycle.

It is observed from Fig. 3-6 that it is possible for i_{L2} to become negative. This requires current to flow in the reverse direction through Q_2 . In order to generalise this phenomenon, it is possible to process Eq. 3-7. It is evident from inspection of Fig. 3-5(c) that, if there is no coupling between the inductors, then a reverse current will never flow; k_c is further used as a handle to analyse the phenomenon, where $M = k_c L$. Eq. 3-7 is differentiated with respect to time and equated to zero. This determines at what time the current is at a minimum. Once this time is found, it is substituted back into Eq. 3-7 and the resultant equation is

$$I_{B_MIN} = \frac{IS_v}{4R_L} \left(\frac{1-k_c}{1+k_c} - 1 - \frac{1-k_c}{1+k_c} \cdot \ln \left(\frac{1-k_c}{1+k_c} \right) \right). \quad 3-11$$

This equation determines the maximum negative current that will flow.

As the designer is interested in where the minimum $I_{B_MIN} = 0$, we can equate Eq. 3-11 to zero and solve for k_c . Thus it is apparent that this phenomenon is a function of the coupling factor k_c alone. However, with reference to Fig. 3-7, it is observed that for any coupling whatsoever, a negative current will result. The current is normalised to $\frac{IS_v}{4R_L}$. For $k_c = 0.9$ (roughly) for the prototype, $I_{B_MIN} = -9$ A,

according to this equation; Fig. 3-6 shows good agreement with this approximation

The prototype is constructed using IGBTs with built-in anti-parallel diodes so current will be allowed to flow with no adverse effect on system operation. If no path was open for current to flow, a negative voltage across the IGBT would develop.

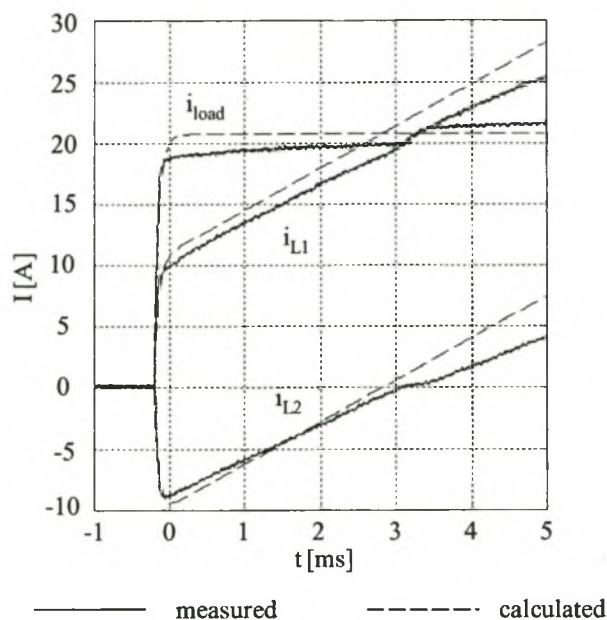


Fig. 3-6 Measured vs calculated results for the initial transient

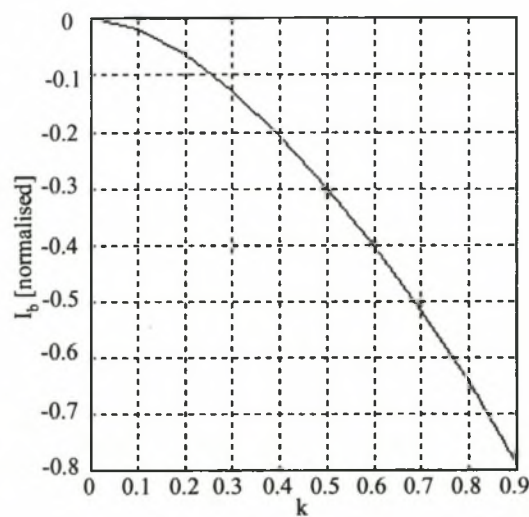


Fig. 3-7 Negative charge current vs coupling factor k_c

Steady state-charge cycle

The steady-state charge cycle is calculated assuming that no load current flows during the charge cycle. The charge cycle equation is simply

$$IS_i = \frac{IS_v}{L_{ESR_TOT} + IS_{ESR}} \left(1 - e^{-\frac{L_{ESR_TOT} + IS_{ESR}}{L_{ST}} t} \right), \tag{3-12}$$

where $\frac{L_{ST}}{L_{ESR_TOT} + IS_{ESR}}$ is defined as t_{const} . This parameter is used extensively in the optimisation procedure. To include the effect of the small load current (of steady-state $\frac{IS_V}{4R_L}$ from Eq. 3-8 and 3-9), the current can simply be added or subtracted from Eq. 3-12. The currents will equal

$$IS_i = i_{L1} = \frac{IS_V}{L_{ESR_TOT} + IS_{ESR}} \left(1 - e^{-\frac{L_{ESR_TOT} + IS_{ESR}}{L_{ST}} t} \right) + \frac{IS_V}{4R_L}, \quad 3-13$$

and

$$i_{L2} = \frac{IS_V}{L_{ESR_TOT} + IS_{ESR}} \left(1 - e^{-\frac{L_{ESR_TOT} + IS_{ESR}}{L_{ST}} t} \right) - \frac{IS_V}{4R_L}. \quad 3-14$$

3.5 Turn-off switch commutation generalisation

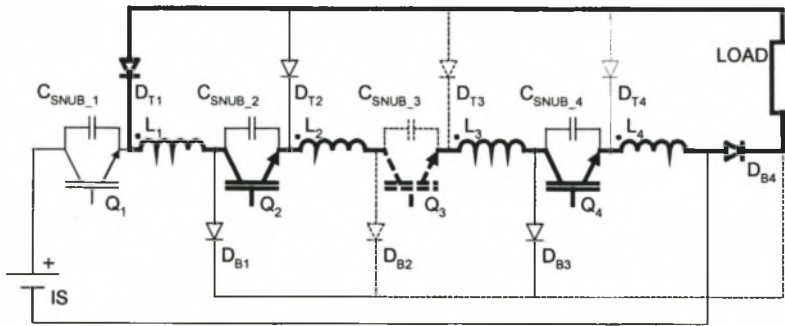


Fig. 3-8 Generalised turn-off commutation

No analysis of the turn-on transient is performed. The full storage inductor effectively acts as a turn-on snubber, so no turn-on switching losses are expected. Fig. 3-8 shows the affected elements for the commutation transient of switch Q_3 . The other transients all follow similar patterns and are not described here. Each commutation transient commutates current out of a turn-off switch and into the two relevant diodes. During commutation, the snubber capacitor will assume the commutated current and it will further determine the voltage rise. The switch model used in this research is a single flank linearly reducing current source (with reference to Fig. 3-9). Once the turn-off device has attained a voltage sufficient to commutate its diode set, the load appears as a resistive load and the relevant circuit description can be utilised.

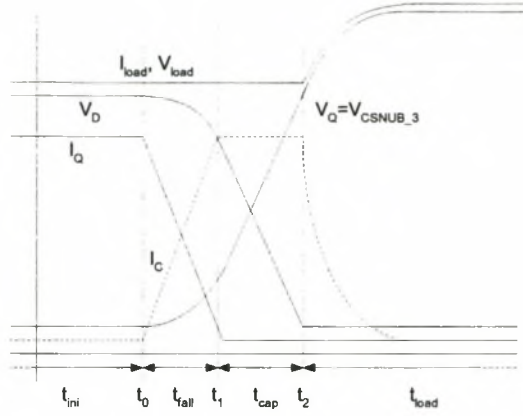


Fig. 3-9 Switching waveforms

Time period $t \leq t_o = t_{ini}$

This period determines the initial conditions of the relevant parameters. Q_3 is on. The diode voltage incorporates $V_{DT3} + V_{DB2}$ as a single quantity, referred to as V_D . $V_D = V_{load}$, $V_Q = 0$ V and $I_Q = I_0$.

Time period $t_o < t \leq t_1 = t_{fall}$

The switch is busy commutating. The current fall is linear through the switch. The load at this stage appears inductive and the total current remains constant at I_0 . The current through the snubber capacitor is equal to $I_0 - I_Q$, which rises linearly. The resultant waveforms for this period are:

$$v_C = v_Q = -\frac{I_0}{2C_{snub_3}t_{fall}}t^2 + \frac{I_0}{C_{snub_3}}t, \quad 3-15$$

$$v_{load} = V_{load}(t_0), \quad 3-16$$

and

$$v_D = v_{load} - v_C. \quad 3-17$$

Time period $t_1 < t \leq t_2 = t_{cap}$

The switch has completed commutation and the snubber capacitor now assumes the full current. Thus $I_C(t) = I_0$. The diodes have not yet commutated. The resultant waveforms for this period are

$$v_C = v_Q = \frac{I_0}{C_{snub_3}} t + V_C(t_1), \quad 3-18$$

$$v_{load} = V_{load}(t_0), \quad 3-19$$

and

$$v_D = v_{load} - v_C. \quad 3-20$$

Time period $t_2 < t < \infty = t_{load}$

Fig. 3-10 shows the equivalent circuit path that develops once the diode voltage $v_D = 0$. The current source represents the storage inductor composed of L_1 and L_2 which discharges into the load at t_2 .

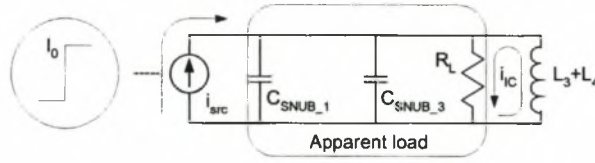


Fig. 3-10 t_{load} discharge model

The load steady initial condition is represented as current sourced from L_3 and L_4 . With reference to Fig. 3-10, it is now apparent that the snubber capacitor is in parallel with the load. Not only that, but C_{SNUB_1} , also in parallel to the load, plays a role in the next transient. Modelling the load therefore as a resistor in parallel with the 2 capacitors, referenced as the compound capacitor C_{com} , the resultant output waveforms equal

$$v_C = v_Q = V_C(t_2) + I_0 R_L \left(1 - e^{-\frac{1}{R_L C_{com}}} \right), \quad 3-21$$

$$v_{load} = V_{load}(t_0) + I_0 R_L \left(1 - e^{-\frac{1}{R_L C_{com}}} \right), \quad 3-22$$

and

$$v_D = 0. \quad 3-23$$

Alternatively, if C_{SNUB_3} is small enough so that the switch is still busy commutating when the diodes forward bias and the resistive load stage begins, the stage referred to as t_{cap} will not take place. Here Fig. 3-10 is still applicable, but the

inductor (initially assumed to be a step current input) will be as depicted in Fig. 3-11. There are no important ramifications under these circumstances.

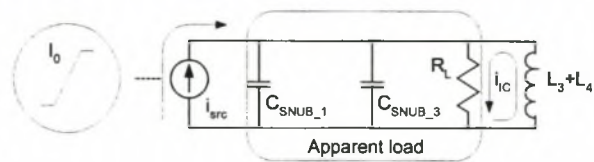


Fig. 3-11 t_{load} discharge model for slow switch times

3.6 Switch cycle discharge paths

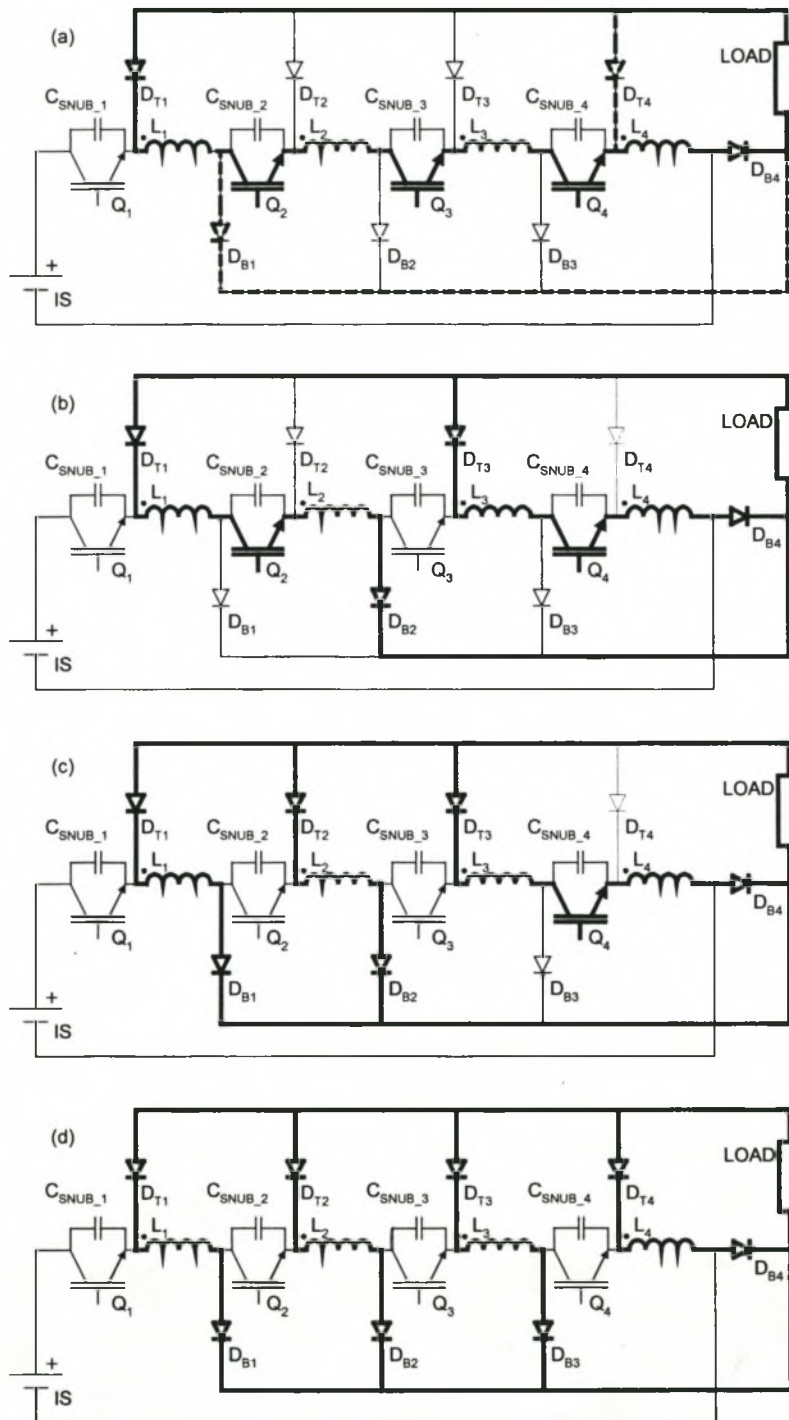


Fig. 3-12 Discharge flow paths for all the switch cycles

First switch cycle Fig. 3-12(a)

The full load discharge paths for the first switching cycle. Switch Q_1 is switched. In bold is the desired discharge path during steady state discharge. In dashed lines is the

extra current path that results from the charge cycle of the new XRAM topology. In this circuit the device anti-parallel diodes, bus capacitor and device parasitics are not shown. The coupling and coupling polarities are shown. Each inductor is coupled to every other inductor.

Second switch cycle Fig. 3-12 (b)

The full load discharge paths for the second switching cycle. Switch Q_3 is switched.

Third switch cycle Fig. 3-12(c)

The full load discharge paths for the third switching cycle. Switch Q_2 is switched.

Fourth switch cycle Fig. 3-12(d)

The full load discharge paths for the fourth and last switching cycle. Switch Q_4 is switched.

3.7 Switch cycle steady-state descriptions

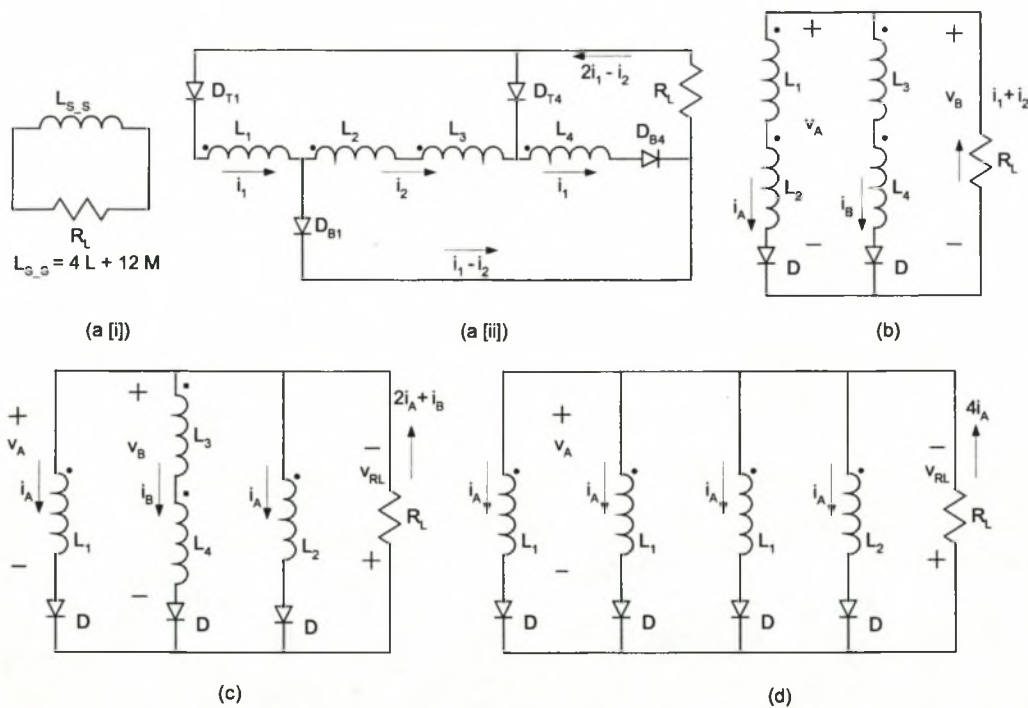


Fig. 3-13 Steady-state equivalents for all the charge cycles

First switch cycle steady state Fig. 3-13 (a)

Fig. 3-13(a[i]) shows the simplified full cycle transient assuming all the switching transients have died out.

The describing equation is simple. The full inductance is the sum of the full inductance matrix \mathbf{M}_n of the form of

$$\mathbf{M}_1 = \sum \begin{bmatrix} L_1 & M_{12} & M_{13} & M_{14} \\ M_{21} & L_2 & M_{23} & M_{24} \\ M_{31} & M_{32} & L_3 & M_{34} \\ M_{41} & M_{42} & M_{43} & L_4 \end{bmatrix} = L_{ST}, \quad 3-24$$

where the sum notation indicates summing of all the terms in the brackets equal to $4L + 12M$ for a balanced system (where L is the single module self inductance and M the mutual coupling between all the modules (which is equal)). If inductor symmetry were not applied, the complete sum of Eq. 3-24 would still result in the full discharge solution; the sum equals L_{ST} . The discharge waveform is of the form

$$i_{load}(t) = I_0 e^{-\frac{R_L + L_{ESR_TOT}}{L_{ST}} t}, \quad 3-25$$

where the inductance ESR is included for the sake of completeness and I_0 is the charge current at the time of commutation. L_{ESR_TOT} is an order less than the load resistance R_L for a typical system (section 5.9) and as a result will dissipate just under 10% of the full stored energy. This would be a point of concern if this was the only discharge state, but as described in section 4.5.5, further states (more parallel discharge branches) result in an improved efficiency.

The discharge state of Fig. 3-13(a[ii]) is unique to the use of an unprotected load and the modified XRAM topology. A 500 kJ ETC system must incorporate some form of load protection so that this state does not occur. However, with reference to section 6.7.7, it is clear that this current imbalance has effects on the prototype that require analysis. The effect is quantified in Appendix A. It is observed that after commutation, the currents i_{L1} and i_{L2} converge to a common value; the rate of convergence is dependent on a number of factors (dealt with in Appendix A). Fig. 3-14 shows measured and calculated results for the prototype with system values of $R_L = 2.6$ (from correlation with section 6.7.4), $L = 2$ mH, $k_c = 0.96$ and $I_{ref} = 52 / 30$. The two graphs are in good agreement. The rounding evident in the measured result is

as a result of the snubber capacitors; spice simulations using snubber capacitors (not shown here) exhibited similar tendencies.

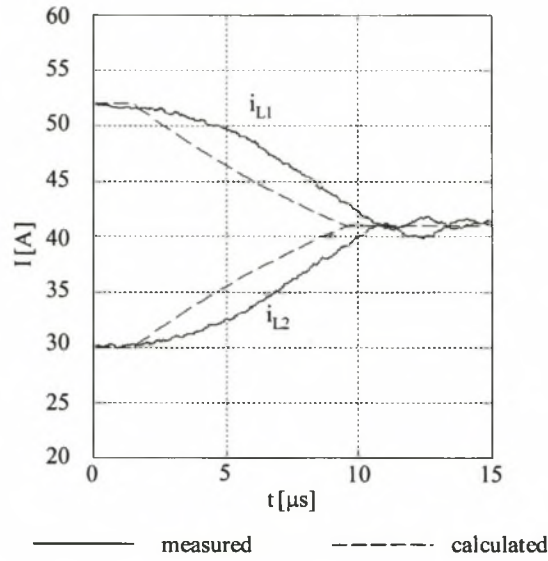


Fig. 3-14 First switch cycle measured inductor balance

Second switch cycle steady state Fig. 3-13(b)

The second switch state inductance matrix is calculated through a further decomposition of \mathbf{M}_n to match the circuit of Fig. 3-13(b). The decomposition is

$$\mathbf{M}_2 = \begin{bmatrix} \sum \begin{bmatrix} L_1 & M_{12} \\ M_{21} & L_2 \end{bmatrix} \\ \sum \begin{bmatrix} M_{31} & M_{32} \\ M_{41} & M_{42} \end{bmatrix} \end{bmatrix} \sum \begin{bmatrix} M_{13} & M_{14} \\ M_{23} & M_{24} \end{bmatrix} \begin{bmatrix} L_3 & M_{34} \\ M_{43} & L_4 \end{bmatrix} = \begin{bmatrix} L_A & M_{AB} \\ M_{BA} & L_B \end{bmatrix}, \quad 3-26$$

where $M_{AB} = M_{BA} = M$. The describing equations for this circuit are

$$v_{load} = R_L (i_A + i_B), \quad 3-27$$

$$v_A = L_A \frac{di_A}{dt} + M \frac{di_B}{dt} + R_{ESR} i_A, \quad 3-28$$

and

$$v_B = L_B \frac{di_B}{dt} + M \frac{di_A}{dt} + R_{ESR} i_B, \quad 3-29$$

where

$$v_B = v_A = -v_{load}, \quad 3-30$$

and $R_{ESR} = \frac{L_{ESR_TOT}}{2}$ is the equivalent series resistance of each branch (this is not shown in the equivalent circuit diagram). The solution of this equation for a balanced system where $L_A = L_B = L$ (and including the internal resistances) is

$$i_A = i_B = I_0 \cdot e^{-\frac{2R_L + \frac{L_{ESR_TOT}}{2}}{L+M}t} = I_0 \cdot e^{-\frac{R_L + \frac{L_{ESR_TOT}}{4}}{\frac{L_{ST}}{4}}t}, \quad 3-31$$

where I_0 is the initial current condition of the two branches (assumed equal). This can be directly obtained from Eq. 4-52 for what is effectively a two-module system. The load current is equal to

$$i_{RL} = 2i_A, \quad 3-32$$

which clearly indicates the reduced dependence of the discharge cycle on the ESR of the inductor.

It is possible that the two branch inductors will not be perfectly balanced. As a result, some form of imbalanced discharge could result. This is discussed in Appendix B. For a 500 kJ system, an inductor value imbalance of 10% results in a current imbalance between branches of 10% in 2.7 ms; as a result, the switching of the next stage should occur at least within this time frame. This may be of concern to the designer and must be taken into consideration.

Third switch cycle steady state Fig. 3-13

The third switch state inductance matrix is calculated through a further decomposition of \mathbf{M}_n to match the circuit of Fig. 3-13 (c). The decomposition is

$$\mathbf{M}_3 = \begin{bmatrix} L_1 & M_{12} & \sum [M_{13} & M_{14}] \\ M_{21} & L_2 & \sum [M_{23} & M_{24}] \\ \sum [M_{31} & M_{41}] & \sum [M_{32} & M_{42}] & \sum [L_3 & M_{34}] \\ & & & M_{43} & L_4 \end{bmatrix} = \begin{bmatrix} L_1 & M_{12} & M_{1B} \\ M_{21} & L_2 & M_{2B} \\ M_{B1} & M_{B2} & L_B \end{bmatrix}, \quad 3-33$$

where $L_1 = L_2 = L_A$ from symmetry arguments in a balanced system. Of interest to the designer in this section is the discharge imbalance that will occur due to the forced inductor imbalance. From the preceding section and Appendix B it is observed that even a slight inductor imbalance can cause an appreciable discharge imbalance. The equations

$$v_{load} = R_L(2i_A + i_B), \quad 3-34$$

$$v_A = (L + M) \frac{di_A}{dt} + 2M \frac{di_B}{dt}, \quad 3-35$$

and

$$v_B = 2(L + M) \frac{di_B}{dt} + 4M \frac{di_A}{dt}, \quad 3-36$$

where

$$v_B = v_A = -v_{load}, \quad 3-37$$

are solved to give

$$i_A = \frac{I_0}{5L - 3M} \left(-L - 3M + 6Le^{\frac{1}{2} \frac{R_L(5L-3M)}{(L+3M)(L-M)} t} \right), \quad 3-38$$

$$i_B = \frac{I_0}{5L - 3M} \left(2(L + 3M) + 3(L - 3M)e^{\frac{1}{2} \frac{R_L(5L-3M)}{(L+3M)(L-M)} t} \right), \quad 3-39$$

and

$$i_{load} = 3I_0 e^{\frac{1}{2} \frac{R_L(5L-3M)}{(L+3M)(L-M)} t}, \quad 3-40$$

where the ESRs are ignored and I_0 is the inductor current (assuming all are the same) at the time of switching. Of particular interest, however, is the rate at which this imbalance will occur. The same procedure as described in Appendix B is used to model the transient imbalance.

The current imbalance $I_\delta = \frac{i_A(t) - i_B(t)}{I_0}$ is calculated to generate a closed

form solution to indicate at what time t_δ this imbalance of current I_δ will occur. The solution is

$$t_\delta = \frac{L - 2L(3k_c^2 - 1 - 2k_c)}{R_L(-5 + 3k_c)} \left(-\ln(3) + \ln \left(\frac{9k + 3 - 5I_\delta + 3k_c I_\delta}{3k_c + 1} \right) \right), \quad 3-41$$

where the substitution $M = k_c L$ is made. For values assumed from section 5.9.4 a 10% imbalance occurs after 50µs! This is fast, but is expected. Fig. 3-15 displays the relation of t_δ to k_c for a 10% current imbalance and of I_δ for $k_c = 0.85$. It is observed that $i_A = 0$ after just over 600 µs. It is thus clear that switching of only Q_2 will result in a fast current imbalance. For balanced discharge waveforms (for a coupled system), it would appear therefore that this state should persist for as short a time as possible, if

at all. This is determined by the final system requirements. Analysis of the results described in this and the preceding section show that it is undesirable to have an inductor imbalance within the circuit; also, it is observed that module coupling aggravates the current imbalance that occurs.

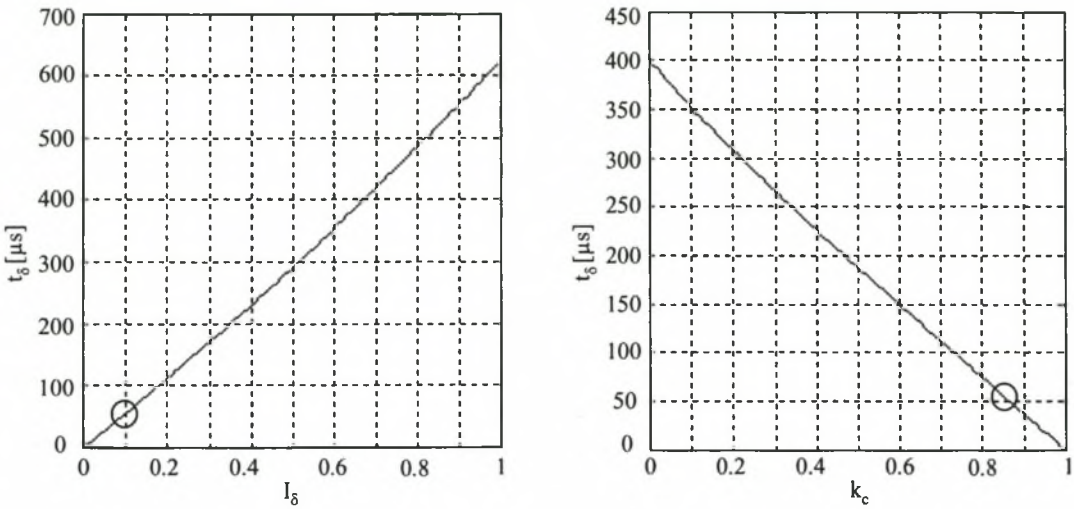


Fig. 3-15 k_c and I_δ vs t_δ for switching of switch Q_2

Depending on the load requirements, a short current spike that will result from an imbalanced discharge may be useful in the way of pulse shaping. However, a full module’s switch hardware is required to generate such a spike. Effective use of such an imbalance is possible, but would require tailoring of the coupling factor and the additional hardware requirement; as a result the system is no longer volume-optimised.

It would appear therefore that the fourth stage – which again balances the discharge – should be switched in as soon as possible. Of interest to the designer is the maximum allowed time (defined by the system parameters and allowed current imbalance) and the duration and magnitude of the transients that could also occur in this time frame. Eq. 3-41 can be used to calculate the allowable time delay.

Fourth switch cycle steady state Fig. 3-13

No decomposition of \mathbf{M}_n is required. The matrix

$$\mathbf{M}_4 = \begin{bmatrix} L_1 & M_{12} & M_{13} & M_{14} \\ M_{21} & L_2 & M_{23} & M_{24} \\ M_{31} & M_{32} & L_3 & M_{34} \\ M_{41} & M_{42} & M_{43} & L_4 \end{bmatrix}, \quad 3-42$$

describes the magnetic circuit fully. For a balanced system, analysis of the equations as performed in the preceding sections is performed or Eq. 4-52 can be used to calculate

$$i_{RL} = 4I_0 e^{-\frac{4R_L + \frac{L_{ESR_TOT}}{4}}{L(1+3M)}t} = 4I_0 e^{-\frac{R_L + \frac{L_{ESR_TOT}}{16}}{\frac{L_{ST}}{16}}t}. \quad 3-43$$

The describing equations of a full unbalanced system are calculable, but little useful information can be derived from them; specific imbalance cases can be analysed if required. Information regarding the sensitivity of the output waveforms on small inductance value deviations can be related to the situation described in Appendix B and large value deviations to that presented in the third switch state discussion. Numerical analysis can be used to model the system further.

3.8 Switch cycle commutation and overshoot descriptions

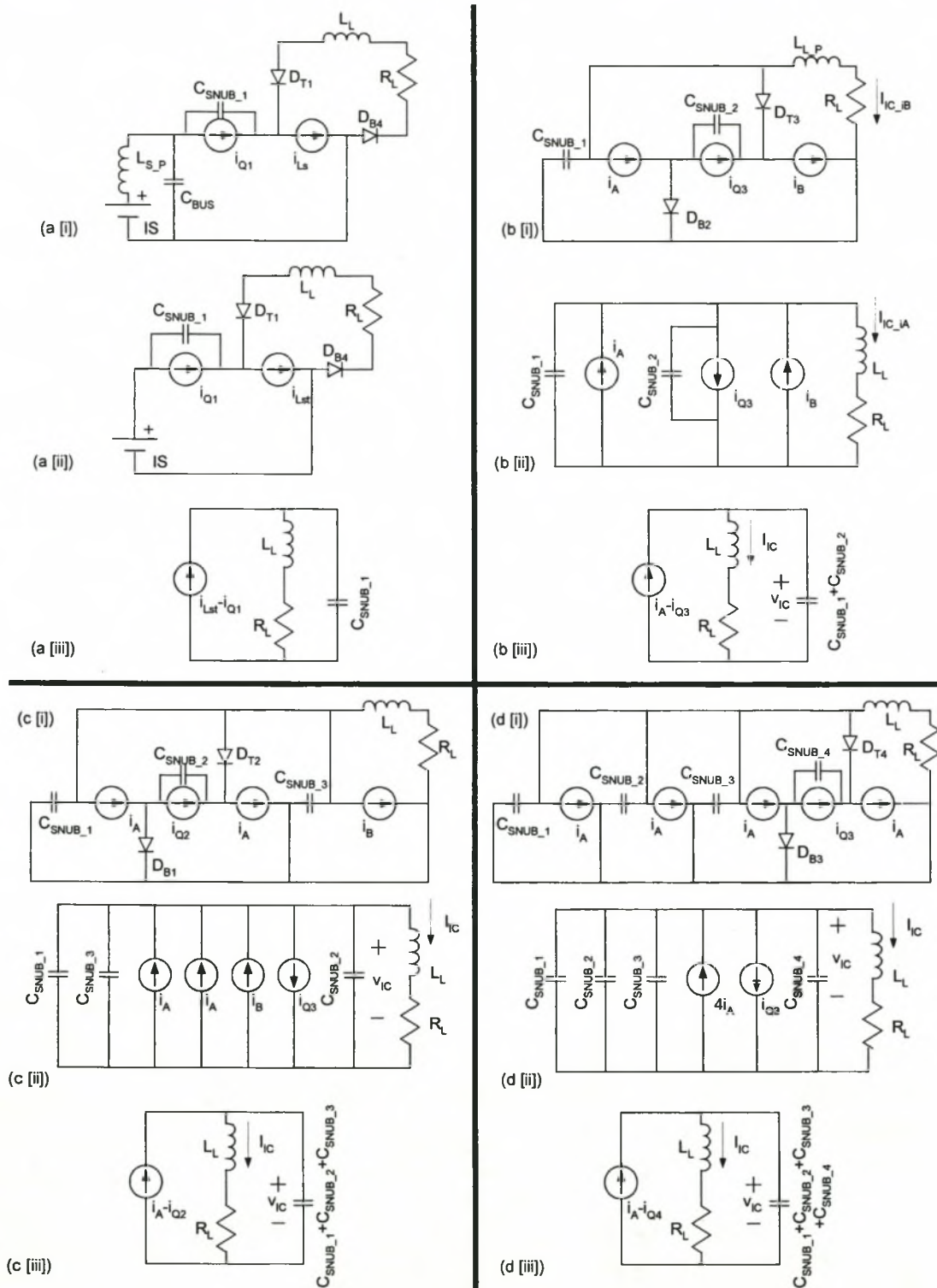


Fig. 3-16 Overshoot considerations for all the switch cycles

3.8.1 Overview

The commutation of an inductive source into a load using high di/dt s requires careful analysis of the conduction paths and commutation waveforms in order to quantify the possible voltage overshoots that could result. This section provides a general analysis of each switching transient and recognises the relevant current magnitudes that are switched and what current paths are affected, including the effect of possible load inductances. The ‘steady-state’ transients are generalised in the preceding sections. Here the storage inductors are modelled as current sources.

Each commutation is presented in three stages of analysis. The first, designated by a (i), is the actual circuit showing the components of concern and replacing the switch and the storage inductors with current sources. The second, designated by a (ii), is the simplified representation of (i) and establishes the parallel paths that are applicable. The third, designated by a (iii), is the final model used in each transient examination. Where applicable, initial conditions are shown. Of interest to the designer is the magnitude of any voltage overshoot.

The main overshoot concern is that posed by the load inductance, L_L ; the others are ignored or dealt with where applicable. L_L is composed of inductance within the load, in the freewheel diodes and mainly in the cables leading to the load. This last inductance will be minimised through the use of co-axial load cables, but a finite – and appreciable – inductance can still remain if the load is necessarily physically removed from the source. This forms the main stray inductance discussed in the following sections.

Voltage overshoots can be contained through some form of capacitive snubbing or MOV-type protection. This latter is considered a secondary – and only precautionary – measure. The device that requires protection – usually a switch or device isolation – has inherent in it some stray or small capacitance. Energy exchange between any stray inductance in the conduction path and this capacitance results in a maximum voltage across this capacitance. In extreme case where the stray inductance is high, this effect requires regulation (for the small output capacitance of an IGBT as compared to the expected load inductance, it can be understood that the resultant overshoot may be large).

This regulation is performed through complementing this capacitance with a larger-value discrete capacitor (referred to as the over-voltage snubber capacitor). The value of this capacitor determines the resultant voltage overshoot.

3.8.2 Switch cycle overshoot consideration

First switch cycle overshoot considerations

Fig. 3-16(a)

This analysis is aimed at determining the voltage overshoot that occurs across V_{CE_Q1} . This voltage is effectively that across C_{SNUB_1} (with a small spike due to inductance in the snubber path; this is ignored).

If the inductor current has not yet balanced (this is the case; the balancing transient is of the same time-order as the overshoot transient), this model is still assumed to be complete as the average inductor current remains relatively unchanged when the magnitude of the current imbalance is comparatively low. Thus the assumption is made that the current imbalance transient and this transient are independent of one another. It is further assumed that the load current – and thus the load voltage – is zero at the start of the transient. The diodes D_{B4} and D_{T1} only become forward biased when the inductor voltage v_{L_ST} equals IS_V . During this time the switch current is busy falling or has completed falling (assuming a switch transient as discussed in section 3.5) and current is transferred to the capacitor. The capacitor further controls the voltage rise and the inductor begins to freewheel through the load.

As the source current is reduced from the full charge level to zero during the switching of Q_1 , the parasitic contribution of the ESL within the IS and also of the leads leading to the converter (shown as L_{S_P}) is compensated for with the use of a bus capacitor placed close to the converter. This allows the bus capacitor C_{BUS} to be viewed as a short circuit for the full parasitics transient (Fig. 3-16(a[ii])).

With reference to (Fig. 3-16(a[iii])), C_{SNUB_1} has an initial value of IS_V before this model becomes applicable. The derivation of the single current source $i_{Ls} - i_{Q1}$ is

under the assumption the resultant over-shoot (and final voltage settling) is superimposed on this initial condition.

Analysis of Fig. 3-16(a[iii]) shows that the capacitor voltage (and thus the switch V_{CE} which is the parameter of interest) response to a step-input current waveform (in a Laplace domain representation) equals

$$V_{C_SNUB}(s) = \frac{I_{SRC}}{s} \frac{R_L + sL_L}{L_L C_{SNUB} s^2 + R_L C_{SNUB} s + 1}, \quad 3-44$$

which appears as a second-order response equation to the step input. However, for typical system values the zero at $-\frac{R_L}{L_L}$ is not negligible, and standard voltage overshoot, rise time and settling time approximations as discussed in [78] are not valid. A rough worst-case equation (described in Appendix C) of

$$V_{C_PEAK} = I_{SRC} R_L + I_{SRC} \sqrt{\frac{L_L}{C_{SNUB}}}, \quad 3-45$$

can be processed as a quick check. However, accurate voltage overshoot predictions must be made through a full transient simulation using a relevant package (Spice is used in this project).

Second switch cycle overshoot considerations

Fig. 3-16(b)

This analysis is aimed at determining the voltage overshoot that occurs across V_{CE_Q3} . This voltage is effectively that across C_{SNUB_3} (with small spikes due to inductance in the snubber path; this phenomenon is ignored in the analysis). However, the same overshoot occurs across V_{CE_Q1} as well.

This analysis is analogous to that of Fig. 3-16(a), with two major differences. Firstly, the inductor source i_{LB} remains constant throughout the transient. It is represented in Fig. 3-16(b[iii]) by an initial current through L_L and a voltage drop across C_{SNUB_3} and the load of $i_{LB} R_L$ as indicated in by V_{IC} . The voltage overshoot that does occur is simply superimposed on this initial condition. Secondly, it is observed that the snubber capacitor C_{SNUB_1} of the first switch cycle is in parallel to C_{SNUB_3} . As a result, these capacitor values are added to form C_{COM} and the resultant

voltage transient is likewise reduced. It is desirable thus to reduce the stray inductance between the connections of these two capacitors; this is shown clearly in the design of the prototype.

Third switch cycle overshoot considerations

Fig. 3-16(c)

This analysis is aimed at determining the voltage overshoot that occurs across V_{CE_Q2} . This voltage is effectively that across C_{SNUB_2} (with small spikes due to inductance in the snubber path; this is ignored). This analysis is analogous to that of Fig. 3-16 (a) and (b). The same overshoot occurs across V_{CE_Q1} and V_{CE_Q3} .

All the sources are parallel to one another, the load and the snubber capacitors. The inductor source i_{LB} and one of the i_{LA} branches are constant throughout the switch transient. The sources i_{LA} and i_{Q2} are combined into a single source analogous to that of the former section but with an offset equal to the $i_{LB} + i_{LA}$; furthermore, the current $i_{LB} + i_{LA}$ is represented as an initial condition in the load path.

The snubber capacitors have an initial voltage of $2R_L I_0$. The magnitude of the new equivalent capacitance results in a reduced effective overshoot, as the capacitors are all parallel to one another and add up to form C_{COM} as the switching sequence progresses.

Fourth switch cycle overshoot considerations

Fig. 3-16(d)

In general this is the important transient as the steady state-offset is potentially the highest at this point. The transient must be predictable. The same process as discussed in the preceding subsections is used. The same overshoot occurs across V_{CE_Q1} , V_{CE_Q3} and V_{CE_Q2} .

All the sources are parallel to one another, the load and the snubber capacitors. The initial condition is composed of a current of $3I_0$ through the inductor and a voltage of $3R_L I_0$ across the snubbing capacitors. The magnitude of the new

equivalent capacitance results in a reduced effective overshoot, as the capacitors are all parallel to one another and add up as the switching sequence progresses.

3.8.3 Overshoot snubbing overview

The following points are made in this section:

1. The main parasitic consideration is the load inductance.
2. The snubbing of this inductance is performed using capacitors.
3. The snubber capacitors combine during the switching sequence, resulting in better snubbing for the later switch cycles.

The alternative is to allow for a dedicated load-snubber placed at the junction of the load cables and the converter. However, this decision is system specific. A distributed snubbing method (as applied here) allows the same capacitors to be used as turn-off snubbers, voltage sharers, local-circuit inductance dampers and the required load inductance snubber.

3.9 Local loop oscillations

Fig. 3-17 has parts (b) to (d); there are no local loop oscillation concerns for the first switching cycle.

With reference to Fig. 3-17(b) and Fig. 3-12(b), as the two branches discharge their current in parallel into the load, it is observed that the two branch switches Q_1 and Q_3 are also in parallel to one another. Excitation of the stray inductance in the path between these devices results in under-damped oscillations between the snubber capacitors and this inductance; the only major damping that does occur is through the ESRs of the devices in the oscillation path. Assuming the worst-case situation of zero damping, the resultant voltage peaks will be equal to

$$V_{C_PEAK} = I_0 \sqrt{\frac{L_{C_P}}{C_{COM}}}, \quad 3-46$$

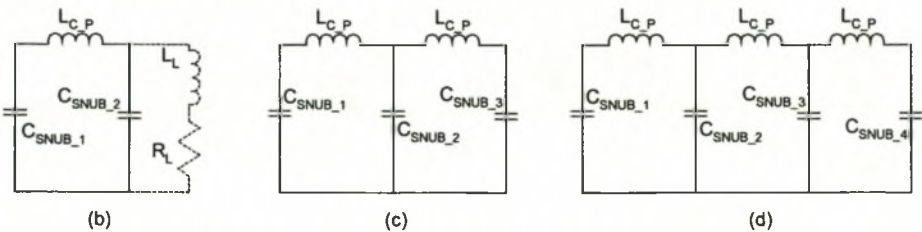


Fig. 3-17 Local loop oscillations

where the compound capacitance C_{COM} is the parallel combination of the snubber capacitors (assumed equal here), I_0 is the commutated current (full branch current at the time of switching), L_{C_P} is a lumped inductance representing the stray inductance of this capacitor loop and V_{C_PEAK} is the additional voltage peak that is superimposed on the existing capacitor voltage (half for each capacitor for equal capacitors). No precautions have been taken in the prototype and it is unlikely any additional damping will be required in a larger system either as L_{C_P} should be as low as possible anyway. If damping is required, a damping resistor either in series or in parallel to the snubber capacitor will be sufficient. Some damping may occur due to the load (shown in dashed lines), but the comparatively large magnitude of L_L effectively shields this high-frequency oscillation from the load.

The other occurrences – those of Fig. 3-17(c) and (d) representing the loops of the third and fourth switch cycles – are similar. A worst-case assumption can be made where the inductances are lumped and the smallest capacitor value is taken and Eq. C-8 used.

3.10 Opening switch thermal issues

A silicon device is thermally characterised by its thermal resistance R_θ , which is used for steady-state temperature calculations, and thermal impedance Z_θ , which is used for the approximation of temperature transients. However, accurate values or models of Z_θ are generally not available and if supplied by the manufacturer are usually very basic and are given as technology specific, not device specific [80].

3.10.1 Device lifetime

Thermal considerations of silicon devices generally fall into two classes. The first is concerned with the device lifetime as a function of its history. This is further separated into ‘intermittent operation’, which deals with temperature transients concerned with system operation (such as the turning on and off of a converter), and ‘power cycling’, which is characterised by short thermal excitation times (10 s or less) and generates results concerning short time-span over-excitation of a device (for fault current testing, for instance). Both are concerned specifically with the device lifetime and charts are supplied in datasheets documenting an expected lifetime depending on

the temperature increase. Correspondence with Mitsubishi gives a rough estimate of a lifetime of 300 000 for a transient of 60°C and 2 000 000 for a transient of 40°C (for their trench gate technology series).

3.10.2 Thermal breakdown

The second thermal consideration is that of thermal breakdown, which occurs when the device exceeds its maximum rated junction temperature (generally at a value of 125°C). This is of distinct importance in this application as it determines the maximum charge current per device.

Diodes and SCRs generally have a documented I^2t rating, giving a maximum allowable current for a 10 ms pulse excitation. This characteristic is not supplied for turn-off devices.

Furthermore, over-current driving of turn-off devices is also device specific. GTOs are sensitive to over-currents as the gate cannot turn off anode currents exceeding a certain maximum value [74]. IGBTs are sensitive to over-currents due to latch-up, although this problem appears to have been solved in newer devices [74].

Analysis of the thermal transient curves supplied in data-sheets to derive general results is possible. The process and an example are given in Appendix D. Correlation of this model's results to a simple RC approximation results in an effective device temperature time constant of around 60 ms. As a check, it is now clear why the generally quoted over-drive time is 10 ms. The design of a system using the suggested volume models of 3.1 for a charge time of 10 ms results in a system volume far exceeding volume requirements. For an exponential charge for a time of 200 ms or more, it would intuitively follow that the junction temperature follows the charge current as if in constant steady state. An assumption is made here that defines the maximum current of a device as

$$Q_I = \frac{\Delta T_{jc}}{R_{\theta} Q_{V_ON}}, \quad 3-47$$

where $\Delta T_{jc} = 125^\circ\text{C} - (T_a + \Delta T_{sa} + \Delta T_{cs})$ and the subscripts *a* refer to ambient, *s* to heatsink and *c* to IGBT package casing.

It is therefore assumed that the device is constantly in a thermal steady state.

A measurable device parameter that supplies information about the junction temperature can be adopted to calculate the actual junction temperature. This can be

the device on-state voltage drop, device threshold voltage, device saturation current or device breakdown voltage (not very useful that one) [61]. The usefulness of this in-time measurement is limited as the parameters are not very thermally sensitive. An alternative approach is to model the device beforehand and pre-define a maximum allowed current and maximum charge time (this is roughly the approach used here).

Ref. [61] suggests and documents a modelling method through controlled tests of an actual device. For the construction of a final system, this analysis should be performed to accurately determine the thermal response – and thus the limitations – of the actual device to be used. Appendix D elaborates this consideration.

The result of this analysis clearly indicates that it is not possible to overdrive turn-off switches in volume optimised long-charge time systems. A possibility is to reduce the device's junction temperature to allow for a larger allowable temperature range during the charge cycle. As the devices would be at ambient temperature before the cycle anyway, some active cooling system – at an extra volume cost – would be required.

The assumption is made here that the maximum current is calculated from thermal resistance values and allowable temperature cycles, using the ambient temperature as the starting point. This current value may differ from that rated for the device. Switch units are further paralleled to allow for the full current rating.

3.11 Opening switch voltage-sharing issues

3.11.1 Foreword

The prime switch requirements for this system are reliability and volume constraints. Also, the inductive storage system has electrical requirements quite different from conventional converters. Where applicable, this difference is highlighted. No single device can match the high power level requirements of typically 20 kV 40 kA, and device serialisation and paralleling is required. This consideration is re-evaluated in the final chapter. Voltage sharing between series-connected devices has received a great deal of attention [62]-[71]. These methods are presented in a comparative flow-chart format and discussed further in Appendix E.

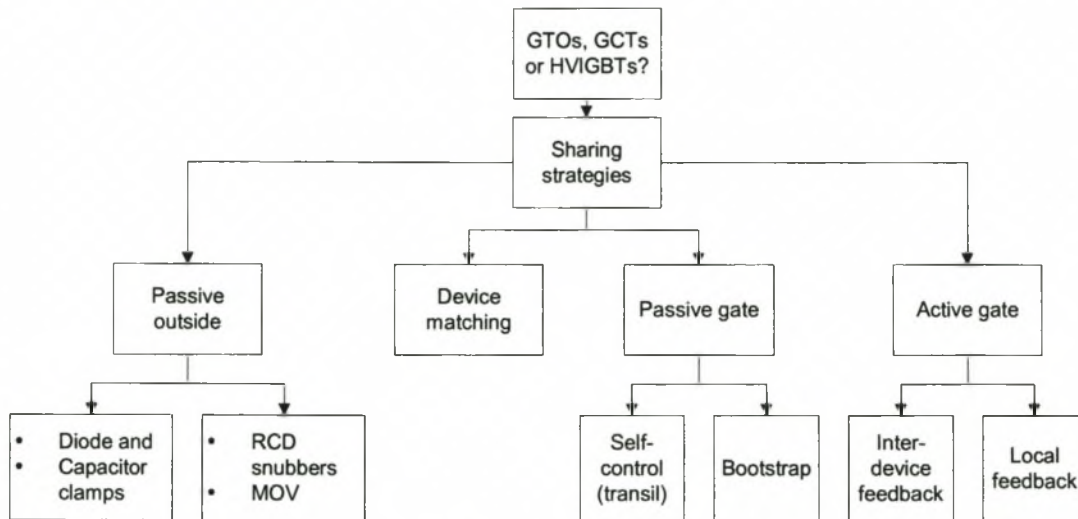


Fig. 3-18 Series sharing strategies

3.11.2 GTOs, GCTs or HVIGBTs?

GTOs

GTOs are high-power devices. They are characterised by high-power gate-drive requirements (typically more than 20% of the device current rating), large snubber requirements and slow switching times. They are used where turn-off devices for frequencies less than 1kHz are required. Mitsubishi markets a device rated at 6 kV 4 kA [72]. References [62] and [63] document voltage-sharing methods of 2-level and 3-level device GTO converters respectively. The voltage sharing is achieved through careful design and matching of the gate drive circuits, GTO device matching and large passive snubbers. Both references provide practical measurements. Ref.[64] documents a conceptual design of a series-stacked GTO-based CSC (controlled series capacitor) application; device and gate-drive matching and snubber capacitors are also used.

IGCTs

Reference [65] compares the performance of high-power IGBTs (HVIGBTs) with the performance of IGCTs in a 250 Hz / 500 Hz traction application. Steffen *et al.* consider IGCTs to provide superior performance for systems rated at 300 kVA – 10 MVA where no device serialisation is required (Steffen documents that equivalent system ratings using HVIGBTs prove less reliable). This article also states that ‘the simple and robust series connection of IGCTs will extend the power range ... to

several hundred megavoltamperes', although this claim is not substantiated. IGCTs are manufactured with dedicated gate drives and as a result no gate-control algorithms can be implemented. It appears therefore that serialisation of the devices will need to be performed through some passive method (although this facet has not been further researched); the resultant volume increase compared to the HVIGBT equivalent is appreciable.

Mitsubishi markets a 4.5 kV 3.2 kA device [72]. This technology, despite its promise, is not considered further.

HVIGBTs

The recent availability of very high-power IGBTs with ratings of 6.5 kV 600 A means that IGBTs, or HVIGBTs, are a definite contender. IGBTs are characterised by simple gate drives, low snubbing requirements and fast switching. Furthermore, it has been documented that successful device serialisation through gate control is possible, with little or no volume increase of the driver itself. So, although the device count itself is higher than contending devices, the total switch volume is potentially lower. A technology comparison table for a 500 kJ system is given in section 5.9.

Furthermore, device paralleling is still an issue. NPT IGBTs have a positive temperature coefficient and can be easily paralleled. GTOs and GCTs, however, are bipolar devices with the related negative temperature coefficient problems.

3.11.3 Suggested voltage-sharing method

Appendix E presents and discusses the relevant voltage-sharing methods currently being used in industry and also those that are relatively new and not widely applied yet (in particular the active gate-control methods).

For the prototype, robust capacitor-only snubbing is performed.

Fig. 3-19 displays the effective sharing hardware used for a 3-element switch. The capacitor value is chosen to compensate for the maximum expected switch delay, t_{delay} . This value is associated with a maximum allowable voltage difference between the highest V_{CE} and the lowest, referenced as V_{DIF} . The delay t_{delay} must incorporate switching differences of the devices themselves, delays caused by the gate drives and potential control delays. A worst-case assumption can be made that adds the full device switching time to t_{delay} and afterwards assumes the switch switches

instantaneously; this makes the capacitor value effectively independent of the device switch waveform. Thus $t_{delay} = t_{controller} + t_{driver} + t_{Q_off}$.

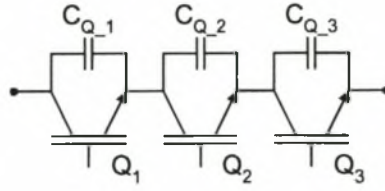


Fig. 3-19 Three-device serial connection

For long commutation times, this approach is impractical and device waveforms will have to be brought into consideration. Assuming worst-case assumptions, however, the required capacitor value per device can be calculated with

$$C_Q = \frac{I_Q t_{delay}}{V_{DIF}}, \quad 3-48$$

where I_Q is the current the device is conducting at the time of commutation. If one device was to switch, say Q_1 , and then the other two only t_{delay} later (this is the worst case situation), then the respective voltage differences between the devices would be $V_{CE_2} - V_{CE1} = V_{DIF}$ and $V_{CE_3} - V_{CE1} = V_{DIF}$. It is clear therefore that the value of the required capacitor is independent of the level of serialisation. This capacitor value is calculated independent of any other snubbing capacitor requirements (such as turn-off or over-voltage snubbing).

The voltage-sharing method employable on a 500 kJ system will invariably have to assume another form, however, as the additional volume requirement of the snubber capacitors is excessive. Many different sharing methods have been proposed in the above sections. In order to choose the one most applicable to this project, let us re-examine the required switch behaviour.

The switch requirements of the XRAM topology allows a very protracted switching cycle as the system switches only once per cycle (every 10 s). As a result, switching losses can substantially exceed those allowed for standard topologies (assuming that sufficient thermal control is exercised). Using the active gate control scheme with separate voltage references that are slowed sufficiently to ensure stable and controlled transients should result in a solution that requires no additional volume when compared to a standard gate drive circuit. An additional advantage of this is that

the slower expected di/dt 's reduce the effect of the parasitic inductances on voltage overshoots.

3.12 Inductor fringe fields, construction and other issues

3.12.1 Back-end transfer efficiency

A number of considerations regarding the inductor have been omitted, for various reasons, in this research. Back-end transfer efficiencies are highly dependent on discharge times and on the inductor construction geometries. This is dealt with in Ref. [9] and requires in-depth specific case analysis.

The research presented in this thesis aims at the broader issues of system and as a result no special-case analyses are attempted.

Ref. [9] uses FEM analysis on single layer PCC and JRC-type Brooks coils. The result is important – for PCC coils the transfer efficiency is less than 80 %, excluding the DC losses. It is clear therefore that this research is a required facet of the full system design. The application of multiwinding coil of a modular system will increase this efficiency significantly; the losses were mainly due to the storage fields coupling with the transverse PCC plates used in the analysis of [9]. This situation is not applicable to multi-layer coils.

3.12.2 Fringe fields

Furthermore, the effect of the inductor fringe fields or indeed the use of the inductor core as storage space is not considered here (it is assumed that the inductor core is empty). Ref. [10] does, however, state that 'in experiments, we never encountered EMI that could not be coped with by conventional methods'. Also, Refs [10] and [12] (Soreq's work) do consider the inductors air-core as storage space.

As the switching transients need not be too fast the main danger is not EMI, but the unpredictable effect of a substantial magnetic field (effectively DC) on other components. No literature has been found that documents the effect of this on solid-state switches, for instance. Its effect on vacuum-type switches is well understood and can be compensated for. This is clear from the VS placement in an effectively field-free (or at least parallel to the direction of charge flow) that is required in a high energy installation. However, the complex construction and charge flow paths of IGBTs or equivalent switches may render this precaution ineffective. Ultimately, this

phenomenon is not well understood and still requires dedicated research. This is further discussed in Chapter 8.

A number of specific literature cases exist where the fringe field, as opposed to its effects, is directly addressed and compensated for. Kanter *et al.* themselves suggest an alternative storage device composed of 4 rectangular winding area inductors arranged in a toroidal pattern. The design is not implemented. Ref. [18] documents the construction of a very high-energy toroidal-type coil composed of 6 removable segments; the fringe field is theoretically zero and sufficiently close for practical purposes. Its volume, however, is excessive.

Magneto-motors product [38] documents the construction (and successful operation) of a six-module system utilising six coupled inductors standing upright in a hexagonal formation. No EMI or H-field problems were documented.

3.12.3 Different inductor geometries

In order to retain generalisation of the volume module documented in the following chapters, Ref. [60] documents the effect of inductor geometry on Eq. 4-26. This is reproduced in the form suggested in Ref. [60] as

$$\tau_I = f \frac{6.03 \times 10^{-8}}{\rho_{metal}} \left[\frac{m}{den_{metal}} \right]^{\frac{2}{3}},$$

3-49

where m is the conductor mass and den_{metal} is the material density used here in this form to avoid possible parameter confusion. This is the equation (in its easily derived volume form) used by Soreq. The parameter f is a inductor type modifier and is listed in Table 3-1.

Table 3-1 Coil type vs shape factor

Coil type	Shape factor f
Brooks	1
Solenoid (single layer)	~ 0.1
Toroid	~ 0.3

It is clear therefore that, while the use of an alternative coil-type will result in increased system volume, the continuous volume computation method proposed in section 4.3 is still valid, provided the relevant shape factor is used.

3.12.4 Isolation issues

For a modular system using coupled inductors, it may be required for two adjacent conductors to experience a potential equal to the full load voltage. This is undesirable but unavoidable in well-coupled and balanced inductors of a Brooks coil configuration. The solution is to ensure that sufficient isolation exists between the conductors. This will invariably result in additional volume requirements for the inductor and will require careful inductor construction.

Thus, despite the fact that the system volume is theoretically independent of volume number, practical construction issues will require the module number to be kept as low as possible. This is used as motivation for decisions made in section 3.3.

3.12.5 Construction issues

It is shown in [10] that an inductor of a volume-optimised system using a Brooks coil is sufficiently strong to retain the full laterally directed pressure that occurs in the device when fully charged. Thus construction issues concerning device strength are not a concern. Eq. 4-57 for the 500 kJ inductor described in section 5.9 shows that a temperature rise in the inductor of 6 K per shot can be expected. If the system is to be fired repetitively, some form of heat-transfer hardware may need to be incorporated into the device; this will invariably increase device volume and complicate the construction issues.

3.13 Diode requirements

Power diodes and SCRs are typically supplied with an I^2t rating, which relates to the maximum current allowed for a certain time span, typically given as 10 ms. This time span relates almost directly to that expected for a typical ETC system's discharge cycle as it is only during this cycle that the diodes conduct. This rating is thus well suited in determining diode current requirements. Furthermore, it is clear why capacitive systems – which conduct high currents only during the discharge stage – have comparatively simple switch requirements.

It can be observed through analysis of Fig. 3-12 that the highest hold-off voltage requirement (excluding overshoot) for any of the diodes is half of the load voltage for any switch cycle. It is observed, however, in section 6.7.7 that the diode voltage may exceed these values due to unmodelled effects (in particular the storage

inductors' stray capacitance) that result in resonance of appreciable magnitudes. These effects should also be sufficiently catered for.

Diode forward recovery voltage peaks may play a role during switch transients as the voltage spike they produce will be superimposed on the turn-off switch during commutation; this phenomenon is relatively unpredictable. CAL (controlled axial lifetime) diodes are used in the prototype to minimise this effect.

3.14 System control, controllability and measurement issues

The primary control of a system incorporates the correct switching of the modules at the correct time and fault level handling. Secondary control considerations incorporate such things as isolator control and *IS* battery recharging and are not considered here.

The module switching times can be either predetermined or triggered through a current feedback measurement; implementation of this is under the discretion of the system designer. The first method is possibly the most robust but charging cycles of the same system may change from shot to shot due to *IS* depletion or component heating. It is possible that the load is not effected by small transferred energy deviations; these considerations are system specific and not incorporated into this research. The use of a current feedback measurement is an alternative but requires the extra hardware and is prone to the normal noise and other issues related to instrumentation. This is however the method adopted in the prototype (with a software watch-dog in case the charge cycle persists for too long).

Measurement issues are also a concern and are required in the prototypes and the final product to monitor system performance. However, the voltage and voltage rise times are not impossibly high. Commercially available probes and instrumentation is available for measuring voltage levels of 20 kV and higher (with the respective voltage rise times).

The current sensor requirements may be an issue as the long front-end charge time can be approximated as a very low frequency – possibly 1 Hz or even DC. Thus an appropriate low-frequency or DC measurement device is required. The use of a detection resistor may be limited as the relevant currents are high. This design facet was not followed further in this research.

3.15 Fault protection

3.15.1 Charge cycle abort

It is possible (and probable) that a system may be primed but not fired. As a result, the energy stored in the inductors must be redirected into a dummy load. During such a time it is important that the actual load is in no way initialised.

For the standard XRAM topology this is possible through the inclusion of two CSs, both rated equal to the already utilised CSs. Reference is now made to Fig. 3-2. The first CS must be included in series with L_4 to protect the load from initialisation as L_4 discharges. The next CS must be connected in series with the dummy load; this dummy load set is connected *before* the other additional CS (just after L_4) and the return path is connected just after OS_1 .

For the modified XRAM topology it is obvious from Fig. 3-4 that a full complement of 4 CSs is required to isolate the load, and then an additional CS to include the dummy load. Thus the advantages of the modified XRAM topology fall away if this type of load-abortion mitigation is required. Alternatively, however, use of the modified XRAM topology for ETC loads requires some form of load protection anyway, most probably in the form of a spark gap within the capillary itself. If the initialisation voltage of this spark gap is kept high enough (which should not be a problem) to be above the highest expected voltage across a full dummy load discharge, then only the dummy load CS is required and the modified XRAM topologies volume advantage is retained.

3.15.2 Load failure during discharge

Load failure during discharge is classed as either open-circuit failure or closed circuit failure. Either one could result in the other if arcing or heat explosion results.

Use of the dummy load during a short-circuit failure in such a situation would require commutation out of the load into the dummy load through the use of a full rating OS in series with the load. In this case, a non-reusable switch such as a solid conductor explosive switch or circuit breaker would be sufficient (the switch need not be fast). Alternatively, for short-circuit failure, an option would be to allow the system to discharge into its own ESRs. However, thermal stability of the switches in such a case could not be guaranteed and switch failure may result.

For load open-circuit failure, the dummy load actuation would necessarily have to be fast enough to avoid extreme over-voltages; this is potentially a problem.

It is clear therefore that load failure is a serious consideration for an inductive storage PFN, and could result in full system failure as well.

It should be stated that this is not the case for a capacitive system in most operating conditions.

3.15.3 Device failure

Device failure can occur through breakdown of the inductor isolation, IGBT failure (IGBTs failure is characterised as short-circuit failure) or diode failure (also short-circuit failure) if the failure is voltage induced. Current-induced failure may result in the device's explosion and a resulting open-circuit failure of the specific switch.

With reference to the modified XRAM topology, if any of the *OS*s fail as closed circuits (except *OS₁*), the topology still retains some functionality, but loses the pulse shaping abilities of that specific module. A slow-blow type fuse is required in series with the *IS* to avoid system failure. Open-circuit failure of an *OS* will result in effective commutation of the effected module (current freewheel through the relevant diodes) and should not affect any of the other modules. Open-circuit failure of the diodes could result in other switch failure if the paths are required for inductor freewheeling.

A default fault mode can be thus be defined if the system malfunctions.

1. A low-resistance dummy load is switched in.
2. Switch Q_1 is turned off and the other switches are kept conducting. This will result in a low load voltage and an acceptable discharge time.
3. If an *OS* fails into an open-circuit state, the discharge paths are still stable. If a diode fails under these circumstances, arcing will result.

3.16 Summary

This section presents the standard XRAM topology and suggests and analyses a modified version that requires fewer active switches and results in a lower switch volume. The only additional modification the use of this modified topology requires is that some form of load protection must be incorporated, necessarily within the load if the load is an ET capillary.

It is shown in section 3.3 that a volume-optimised system necessarily requires balanced inductor modules; this assumption is made throughout the circuit analyses. Section 3.3 shows that stable discharge states (where stable is defined as equal discharge gradient in all the modules) require that all the discharge branches are also balanced. A 4-module version of the modified XRAM topology is analysed and it is shown that the circuit will function as expected. Of interest is the fact that switch protection circuitry (the over-voltage protection circuitry) need not be duplicated for each switch as the switches appear in parallel when switched and share the protection circuitry.

A number of special-case considerations have been singled out and general descriptions constructed; none are serious or hamper the overall functionality of the circuit, however.

One of the most important difficulties with inductive storage – that of the thermal excitation of the turn-off switches – is discussed, with focus on the application of solid-state switches. It is made clear that the thermal properties of these switches is not well defined in industry and that applicable switches need to be tested individually to determine their limit criteria. A simple thermal model is discussed in this chapter and it is considered best to not use the switch above its rated current.

As an actual ETC application will invariably require high-voltage switches – on the order of 20 kV – device serialisation will become necessary. This consideration is also covered in this chapter. Lastly, a number of system considerations – namely control, measurement and fault-level handling – are presented.

For the modified XRAM topology to be applicable to this application, it has been shown that it is required for voltage hold-off to be incorporated *within the load* so that current does not flow through the load during the charge cycle or during pre-fire system failure situations. If this is not possible, the standard XRAM topology should be used.

Fault mode handling has also been discussed. It is clear that inductive storage systems are not very forgiving during fault situations. If a fault occurs, it is likely that the current stored in the inductors will either persist long enough to thermal stress the conduction paths, or if the current is interrupted, will result in a voltage high enough to result in isolation breakthrough. It is again stated that capacitive systems are effectively open-circuit safe, a distinct operational advantage.

CHAPTER 4

VOLUME OPTIMISATION CONCERNS

4.1 Introduction

The volume optimisation of an inductive storage PFN involves the optimisation of a number of interdependent sub-system parameters. Refs [10] and [12] document a system design method. This method is assumed in this project (referred to as the continuous model) and is documented here. Where applicable, attention is drawn to where changes or additions to the model of [10] have been made. The continuous model has a number of shortcomings; they are identified and a discrete model is developed that allows for their circumvention.

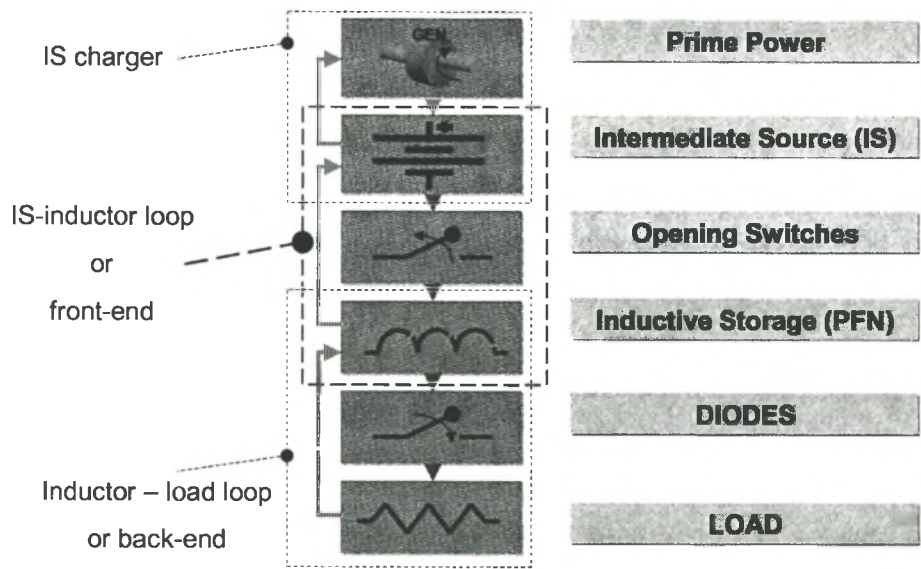


Fig. 4-1 Sub-system identification

The five subsystems are shown in Fig. 4-1. The prime power source (shown as the generator) is used to charge the batteries. This sub-system is not included in the design process. The intermediate storage, or IS, is composed of batteries. The switches (the opening switches and diodes of Fig. 4-1) form a sub-system and are composed of high-voltage IGBTs or HVIGBTs and discrete diodes. The inductor is used as the pulse-forming stage of the circuit and converts the energy delivered from the IS to a form acceptable to the load. The load is approximated as a resistor. This

design utilises a 2-stage system involving firstly the transfer of energy from the IS to the inductor (defined as the front-end) and secondly from the inductor to the load (defined as the back-end). Dimensioning of the prime power source is not considered.

This chapter identifies the parameters available to the designer, defines and discusses the parameter relationships, presents a volume model and discusses and motivates the assumptions that are made.

4.2 Sub-system parameter identification

4.2.1 IS, Battery model

Ref. [10] defines the battery power density s_{BP} as the maximum power delivered to a matched load divided by the device volume. The generalisation of requiring a matched load is avoided by redefining s_{BP} as the device open-circuit voltage multiplied by the device short-circuit current divided by the device volume. The battery peak power S_{BP} is defined (both in [10] and here) as

$$S_{BP} = s_{BP} \text{Batt}_{VOL} , \quad 4-1$$

where Batt_{VOL} is the battery unit volume. The total IS volume is equal to both

$$IS_{VOL} = N_P N_S \text{Batt}_{VOL} , \quad 4-2$$

which is composed of a bank of batteries of N_P parallel units and N_S series units or

$$IS_{VOL} = \frac{S_{ISP}}{s_{BP}} , \quad 4-3$$

where S_{ISP} is the peak power of the whole IS and s_{BP} is continuous and specific to a battery technology. Use of the variable s_{BP} makes the IS volume a continuous function of S_{ISP} . This is utilised in the continuous volume model described in section 4.3.3.

The IS equivalent series resistance IS_{ESR} , IS short circuit current IS_I and IS open-circuit voltage IS_V can be derived from Eq. 4-3 by initially assuming a value of one of these factors. In the discrete volume model discussed in section 4.5, the battery open-circuit voltage $BATT_V$ is assumed and the other factors derived from s_{BP} . The battery model is shown in Fig. 4-2.

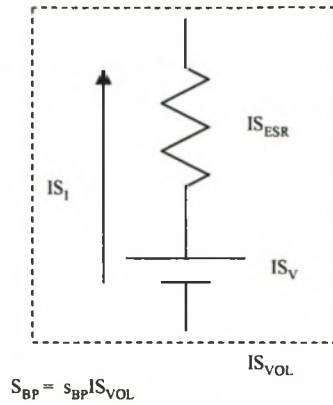


Fig. 4-2 IS model

These parameters are all dependent on a number of factors involving the device's history. This is taken into consideration by defining limits – open-circuit voltage, temperature and energy discharge maximum – and by further assuming that all operation takes place within these limits.

4.2.2 Switches: HVIGBTs (turn-off) and diodes (turn-on) volume model

For device volume optimisation the important parameters are: unit volume, device protection circuitry volume, gating unit volume, switch maximum voltage, switch maximum current and unit heat sink requirements and heat sink volume. Other considerations, such as efficiency, electrical stability and switching behaviour, are dealt with in the relevant sections.

The current-carrying capability of a silicon device during conduction (excluding switching considerations) is determined by four factors: the duration of the conduction time, the magnitude of the current, the devices on-state voltage and the devices thermal impedance characteristic ([74] pp. 731-743). In order to take advantage of the thermal capacity of the device and for a device to conduct more than its rated current, the conduction time should be appreciably less than the device's thermal time constant (discussed in the previous chapter). As this is not the case (refer to section 3.10), a conservative estimate of allowable current over-driving is assumed here.

That is, the device is assumed to be in its thermal steady state immediately following power excitation. As a result, the device has a maximum current determined by the maximum allowable temperature difference above ambient ΔT_{js} (where ambient in this case is the heat sink temperature), instantaneous power dissipation

during conduction P_{cond} and steady-state thermal resistance $R_{\theta js}$. Depending on the charge cycle length t_{CH} , system front-end charge time constant t_{Const} , the firing repetition rate and required charge current maximum I_{REQ} , the average power dissipation can be calculated.

From this, the relevant heat sinking requirements are determined and the relevant heat sink volume according to the applied technology. The full volume per switch unit, Q_{VOL} , is calculated with the addition of the switch volume, gate-drive volume, sharing hardware volume and heat sink volume.

4.2.3 Inductor Volume Model

The inductor is composed of electrically modular units that are magnetically incorporated into a single device. As a result the final device will be a single coil with isolated taps running to the switches and the load. The inductor is a Brooks coil ([73] p. 90) where the name is used to describe the inductors specific geometry. This geometry is suggested in [10] and [12].

A Brooks coil allows the maximum inductance for the shortest length of conductor (thus the maximum time self time constant τ_i). It is characterised by its physical dimensions that are related as follows: its outer radius is double its inner radius and its height is equal to its inner radius. This is shown in Fig. 4-3.

Discrete inductor volume model

For a pre-defined ESR, the Brooks coil results in the maximum achievable inductance for the minimum inductor volume. Grover [73] p. 93 gives the equation

$$L_{ST} = 5 \times 10^{-8} \cdot \frac{l^{\frac{5}{3}} \left(\frac{c}{2a} \right)^{\frac{2}{3}}}{\pi^{\frac{5}{3}} \delta^{\frac{2}{3}}} \cdot P_0' \quad 4-4$$

to describe the relationship between the dimensions of a generalised rectangular winding-area inductor and its self-inductance L_{ST} . The factor l is the conductor length, c the inner radius, a the mean radius, δ the conductor diameter and P_0' , a dimensionless constant dependent on the value of c and a . For the Brooks coil, $\frac{c}{2a}$ is equal to 0.333 and P_0 equals 17.107.

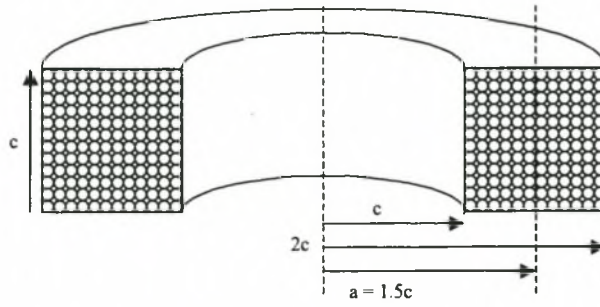


Fig. 4-3 Brooks coil dimensions

Having calculated the required L_{ESR_TOT} of the inductor in the optimisation protocol (discussed at a later stage), the equation

$$l = \frac{L_{ESR_TOT} \cdot \pi \cdot \left(\frac{\delta}{2}\right)^2}{\rho_{metal}}, \quad 4-5$$

is substituted into Eq. 4-4 to obtain

$$\delta = 590.193 \times \frac{\rho_{metal}^{\frac{5}{8}} L_{ST}^{\frac{3}{8}}}{L_{ESR_TOT}^{\frac{5}{8}}}, \quad 4-6$$

where ρ_{metal} is the metal resistivity. Thus with the required inductance L_{ST} and required ESR L_{ESR_TOT} we are able to calculate the required conductor diameter. From this the required winding number and inductor volume can be calculated from the equations

$$N = 174 \cdot \left(\frac{L_{ST}}{\delta}\right)^{\frac{2}{5}}, \quad 4-7$$

and

$$L_{VOL} = 4\pi \cdot N^2 \cdot \delta^3, \quad 4-8$$

with L_{VOL} the full inductor volume including the central air-core. Eqs 4-6 to 4-8 are used in the discrete model presented in section 4.5. Of importance is that with an input of inductance and inductor ESR, it is possible to calculate the full inductor volume.

Not taken into account is the required isolation compensation. This is important as for a modular inductive, inter-winding isolation needs to be the full load voltage, which is on the order of 20 kV. This can be incorporated into the design at a

later stage with the use of a first-principles inductance design calculation (which also serves as a check) described in section 4.2.5.

Continuous model inductor volume model

Also from Grover (p.100) are the equations

$$N = \left(\frac{c}{\delta} \right)^2, \quad 4-9$$

and

$$c = 13.14 \cdot L_{ST}^{\frac{1}{5}} \delta^{\frac{4}{5}}, \quad 4-10$$

where it is observed that the volume is directly related to the dimension c . Combining these equations with those of the discrete model gives an alternative volume relation (documented in [10]) as

$$L_{VOL} = \frac{K}{\rho_{metal}} \tau_i^{\frac{3}{2}}, \quad 4-11$$

with τ_i equal to $\frac{L_{ST}}{L_{ESR_TOT}}$ (the inductor time constant) and K a dimensionless constant.

Eq. 4-11 is used in the continuous model of section 4.5. The value of K differs from publication to publication ([10], [60] and [73] p.101); this is discussed in 5.1.1.

Neither of these models incorporates isolation thickness considerations.

4.2.4 Inductor Electrical Model

System modularity is required in order to allow for sufficient pulse shaping. The volume model is necessarily a function of this modularity. It is in the designers interest to quantify this dependency. The following discussion presents the electrical model of the modular inductor.

Chapter 3 analyses a 4-module modified XRAM topology. It is observed that each discharge state is fully described by the load resistor value, the inductance matrix \mathbf{M}_4 and the stages initial conditions. This section generalises this matrix to incorporate n modules.

The full inductor value L_{ST} is the sum of all terms in the \mathbf{M}_n matrix. This value is required for the volume optimisation procedure discussed in section 4.5 and is calculated from Eq. 4-53. It is intuitive however that a normalised \mathbf{M}_n can be developed, independent of the actual value of the inductance.

From the pulse forming perspective, the calculation of the required \mathbf{M}_n is performed from the analysis of the desired electrical discharge pulse form. This is understandably complicated for a highly modular system. Fortunately, the requirement of a balanced system simplifies this process. The analysis presented here is initially generalised to n modules, however, and does not assume balancing.

The descriptors used are described as follows. In a system with n modules, the maximum number of discharge states is equal to n (sequences from the full series discharge till the full parallel discharge). In state n there are also n branches (equal to the number of modules in full discharge configuration). The descriptor m is used to represent a single discharge state where $1 \leq m \leq n$; in the discharge state m there are also m branches. The descriptors p or q are used to represent a single branch in the discharge state m , where $1 \leq p, q \leq m$.

Each discharge state m represents a new inductor configuration and a recalculation of the discharge equation. The diodes are included in Fig. 4-4 to indicate that there is no electrical energy transfer between modules; all the diodes are assumed to be conducting throughout the discharge cycle. The branch ESRs are ignored at first. This assumption is revisited in section 4.5.5.

In Fig. 4-4 it is clear that

$$-v_{load} = v_1 = v_2 = \dots = v_p = \dots = v_m, \quad 4-12$$

where m is the current discharge configuration, also equal to the number of branches in this configuration, and p is any one of the branches. For branch p with inductor L_p the equation

$$-R_L \cdot \sum_{q=1}^m i_q = M_{1,p} \frac{di_1}{dt} + M_{2,p} \frac{di_2}{dt} + \dots + L_p \frac{di_p}{dt} + \dots + M_{m-1,p} \frac{di_{m-1}}{dt} + M_{m,p} \frac{di_m}{dt}, \quad 4-13$$

describes Eq. 4-12 for v_p . Rewriting Eq. 4-13 for branches $1 \leq p \leq m$ results in m equations of the form of Eq. 4-13 that can be incorporated in a matrix format described by

$$-R_L \cdot \begin{bmatrix} 1 & 1 & \dots & 1 \\ 1 & \ddots & & \vdots \\ \vdots & & \ddots & 1 \\ 1 & \dots & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_m \end{bmatrix} = \begin{bmatrix} M_{1,1} & M_{1,2} & \dots & M_{1,q} \\ M_{2,1} & \ddots & & \vdots \\ \vdots & & \ddots & M_{p-1,q} \\ M_{p,1} & \vdots & M_{p,q-1} & M_{p,q} \end{bmatrix} \begin{bmatrix} \dot{i}_1 \\ \dot{i}_2 \\ \vdots \\ \dot{i}_m \end{bmatrix}, \quad 4-14$$

where p and q equal m and $L_1 = M_{11}, L_2 = M_{22}, \dots, L_m = M_{mm}$. Alternatively, this equation can be written in a standard form

$$\dot{\mathbf{i}}_m(t) = -R \begin{bmatrix} M_{1,1} & M_{1,2} & \dots & M_{1,q} \\ M_{2,1} & \ddots & & \vdots \\ \vdots & & \ddots & M_{p-1,q} \\ M_{p,1} & \vdots & M_{p,q-1} & M_{p,q} \end{bmatrix}^{-1} B_m \cdot \mathbf{i}_m(t), \quad 4-15$$

where B_m is the square ones matrix of order m from Eq. 4-14 and \mathbf{i}_m is the vector of the currents i_1, i_2, \dots, i_m .

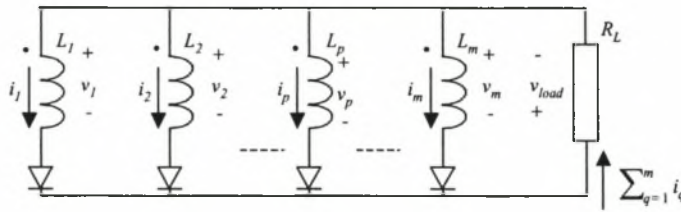


Fig. 4-4 Parallel discharge equivalent for state m

Assuming that a solution to Eq. 4-15 exists, a general solution of the form

$$\mathbf{i}_m(t) = e^{-R_t \mathbf{M}_m^{-1} \mathbf{B}_m t} \cdot \mathbf{I}_m(t_m) \text{ for } t_m \leq t < t_{m+1}, \quad 4-16$$

where

$$i_{load}(t) = \sum \mathbf{i}_m(t) \text{ for } t_m \leq t < t_{m+1}, \quad 4-17$$

describes the full discharge relation for the m -state configuration. $\mathbf{I}_m(t_m)$ is the initial condition vector at the start of the transient at time t_m and \mathbf{M}_m and \mathbf{B}_m are the relevant inductance matrix and ones matrix.

In order to generalise this, the full solution is written as

$$i_{load}(t) = \begin{cases} \sum \mathbf{i}_1(t) = i_1(t) \text{ for } t_1 \leq t < t_2 \\ \vdots \\ \sum \mathbf{i}_m(t) \text{ for } t_m \leq t < t_{m+1} \\ \vdots \\ \sum \mathbf{i}_n(t) \text{ for } t_n \leq t < \infty \end{cases}, \quad 4-18$$

where n is the full number of discharge configurations. The inductance matrix \mathbf{M}_m changes for each configuration. However, \mathbf{M}_n can be decomposed (by the addition of the relevant terms) to generate any of the other discharge states' inductance matrices.

The entire discharge profile can thus be fully predicted by defining a single required inductance matrix \mathbf{M}_n . Furthermore, the requirement of a balancing this

inductance matrix simplifies the normalised inductance matrix until it is composed of only a diagonal of 1's and the rest of the values as equal but necessarily less than one.

4.2.5 Inductor Magnetic model

Using the optimisation method discussed in section 4.5, the full inductor dimensions (Brooks dimension c , conductor diameter δ and winding number N) are determined.

The Brooks coil geometric relations do not need to be exact to obtain maximum inductance [56]. As a result, once the conductor type has been chosen, a relevant winding configuration dependent on the winding number and number of isolated modules can be chosen. Once this is performed, the whole inductor of N windings is described by a characteristic square inductance matrix \mathbf{M}_N of order N .

Each term in this matrix is the mutual inductance of a single winding in the inductor to another winding of the inductor. Quantifying these values with the use of analytical equations as described in [73] becomes very complex. Alternatively, a numerical method using the Biot Savant law in its current stick representation [75] can be used. This is described in Appendix G.

\mathbf{M}_N can be decomposed (described in Appendix G) to generate the required inductor matrix \mathbf{M}_n . The execution of this process is greatly simplified by assuming that \mathbf{M}_n is balanced. The coupling

$$k_c = \frac{M_{p,q}}{\sqrt{L_p L_q}}, \quad 4-19$$

in such a system is equal (or as to close to equal as possible) for all module numbers p and q , where $p \neq q$.

The design process can therefor be summed up in three steps.

1. Firstly, the *normalised* inductance matrix \mathbf{M}_n is calculated knowing only the required module number and that the system is balanced.
2. Secondly, the required full inductor value L_{ST} and inductor dimensions are calculated from the volume module.
3. Lastly, the inductor can be correctly configured through processing of \mathbf{M}_n . This calculation has the added advantage of also double-checking the exact inductance value achievable and allows for the inclusion of the relevant isolation.

4.2.6 Load Model

An analysis of the ETC load is given in section 2.4. It is observed that the discharge current in an ETC load using an inductive source (with apparent inductance seen from the load side as L_{APP}) decays in a finite time of

$$t_{DECAY} = \frac{L_{APP}}{\alpha_{ETC} R_P}. \quad 4-20$$

This project uses the expected discharge time of t_{DECAY} as a design criterion, where the required back-end inductor value (assuming full parallel discharge) is determined according to Eq. 4-20 where t_{DECAY} is required and R_P and α_{ETC} are approximated. This research assumes a value of $\alpha_{ETC} = 1$; a non-unity value for α_{ETC} is trivial to incorporate into the design procedure. Furthermore, the peak resistance approximation R_P is assumed to be equal to an actual resistance of value 100 mΩ for an ETC load [10]. It is assumed that this load resistance remains constant at this value throughout the discharge cycle; the load is further referred to as R_L . Also, it is assumed that pulse forming – and thus modular storage – is required. The level of modularity is discussed in section 3.3.

Examination of the continuous model of section 4.3 shows that no back-end parameters (R_L , α_{ETC} , t_{DECAY} or L_{APP}) play a role in the volume optimisation procedure. However, practical construction concerns of the sub-systems according to the discrete model of 4.4 may require some component re-configuration as a function of α_{ETC} (with no change to overall volume, however).

4.3 Continuous volume model

4.3.1 Model overview

The continuous model describes an analytical volume relationship between the IS and the inductor that allows for a full system volume characteristic equation. This is considered one of the prime design requirements of this project.

An existing model that allows for the optimisation of a single stage system with switch volume and switch effects excluded is described in [10] and [12]. Full understanding of this model is required as it influences and is influenced by a number of design decisions that need to be made. In particular, the model does not fully describe practical system ratings (such as actual IS configuration, back-end pulse

shape matching, the effects of system modularity and sensitivity to switch on-state voltage drop, which is observed to be non-negligible).

It does however allow for the development of a number of useful general results and can be used in conjunction with the discrete model discussed in section 4.4. Section 4.3.2 briefly discusses the results documented in [10] and [12]. Section 4.3.3 expands this model; attention is drawn to where alterations are made.

4.3.2 Existing model

The continuous model adopted in this research is that proposed in [10]. A number of assumptions have been made in [10]. These are listed here.

1. The coil is of aluminium and operates at room temperature.
2. The maximum stress in the coil is below the tensile stress strength.
3. The prime power and the external load impedances (IS and inductor ESR) are matched: $IS_{ESR} = L_{ESR_TOT}$.
4. Interface resistances and inductances are neglected.
5. IS (or battery) maximum delivered power S_{BP} is proportional to its volume IS_{VOL} in the relation $S_{BP} = s_{BP} \times IS_{VOL}$ where s_{BP} is the specific power of the batteries, or battery power density. The specific power is defined here as the maximum deliverable energy to a matched load; this is different from that used in this project as discussed in section 4.2.1.
6. The charging time is $t_{CH} = 2 \times t_{const}$, where $t_{const} = \tau_I / 2 = L_{ST} / (2 \times L_{ESR_TOT})$.

Incorporation of all of these constraints including the volume equation description of

$$\tau_I = \frac{6.03 \times 10^{-8}}{\rho_{al}} \cdot L_{VOL}^{2/3}, \quad 4-21$$

given in [60] where ρ_{al} is the resistivity of aluminium and τ_I the Brooks coil time constant leads to a volume equation of the following form (from [10])

$$V_{VOL_TOT} = \left(\frac{E_{STORED}}{\epsilon_{SOREQ} \cdot S_{BP} \cdot \lambda_r} \right)^{3/5} (1 + \lambda_r), \quad 4-22$$

where

$$\lambda_r = \frac{IS_{VOL}}{L_{VOL}}, \quad 4-23$$

and the other components are constants (described at a later stage). The electrical model of the described circuit is shown in Fig. 4-5.

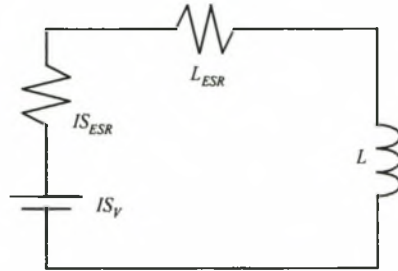


Fig. 4-5 Front-end circuit

4.3.3 Continuous model expansion

The above model is reproduced here. Some changes to this model are made by the author. In particular, assumptions 1, 3 and 6 of the above section are incorporated into the design procedure and it is observed that the results can be generalised.

The new assumptions can be reduced to include only the following:

1. The maximum stress in the coil is below the tensile stress strength.
2. Interface resistances and inductances are neglected.
3. IS peak power S_{ISP} is proportional to its volume IS_{VOL} by the relation $S_{BP} = s_{BP} \times IS_{VOL}$, where s_{BP} is the specific power or power density of the battery technology defined as $BATT_v \times BATT_I$ (open-circuit voltage and short-circuit current, assuming no load) divided by the battery unit volume. This is different to [10] and is purposefully done to include the effect of the front-end ESR relation.

The IS peak power as defined in Eq. 4-3 can be written as

$$S_{ISP} = \frac{IS_V^2}{IS_{ESR}}. \quad 4-24$$

Equating $L_{ESR} = k_{\Omega} \times IS_{ESR}$ with k_{Ω} a dimensionless ESR modifier, the energy stored in a coil at time t_{CH} can be derived as

$$\begin{aligned}
 E_{STORED} &= \frac{L_{ST} I_{REQ}^2}{2} = \left(I_{final} \left(1 - \exp\left(-\frac{t_{CH}}{t_{Const}}\right) \right) \right)^2 \frac{L_{ST}}{2} \\
 &= \left(\frac{IS_V}{L_{ESR} + IS_{ESR}} \left(1 - \exp\left(-\frac{t_{CH}}{t_{Const}}\right) \right) \right)^2 \frac{L_{ST}}{2} \\
 &= \frac{IS_V^2}{IS_{ESR}} \cdot \frac{L_{ST}}{2(k_{\Omega} + 1)^2 IS_{ESR}} \cdot \left(1 - \exp\left(-\frac{t_{CH}}{t_{Const}}\right) \right)^2, \quad 4-25 \\
 &= \frac{IS_V^2}{IS_{ESR}} \cdot \frac{k_{\Omega}}{2(k_{\Omega} + 1)^2} \cdot \frac{L_{ST}}{L_{ESR}} \cdot \left(1 - \exp\left(-\frac{t_{CH}}{t_{Const}}\right) \right)^2 \\
 &= S_{BP} \cdot \tau_I \cdot \frac{k_{\Omega}}{2(k_{\Omega} + 1)^2} \cdot \left(1 - \exp\left(-\frac{t_{CH}}{t_{Const}}\right) \right)^2
 \end{aligned}$$

where $\frac{L_{ST}}{L_{ESR}} = \tau_I$. Eq. 4-21 using [73] gives

$$\tau_I = \frac{3.96 \times 10^{-8}}{\rho_{metal}} \cdot L_{VOL}^{2/3}, \quad 4-26$$

for any metal. Substitution of Eqs 4-24 and 4-26 into 4-25 gives a relation (with some rearrangement) of

$$\alpha = IS_{VOL} L_{VOL}^{2/3}, \quad 4-27$$

where

$$\alpha = \frac{2E_{STORED} \rho_{metal}}{S_{BP} 3.96 \times 10^{-8}} \cdot \frac{(k_{\Omega} + 1)^2}{k_{\Omega}} \cdot \left(1 - \exp\left(-\frac{t_{CH}}{t_{Const}}\right) \right)^{-2}. \quad 4-28$$

The designer is interested in finding the total combined volume VOL_{TOT} defined as

$$VOL_{TOT} = IS_{VOL} + L_{VOL}. \quad 4-29$$

Rearrangement of Eq. 4-29 using Eq. 4-28 gives

$$VOL_{TOT} = \alpha^{3/5} \left(\lambda_r^{2/5} + \lambda_r^{-3/5} \right), \quad 4-30$$

where λ_r is the ratio $\frac{IS_{VOL}}{L_{VOL}}$ (this is very similar to that of [10], with only one or two changes as described).

Some general results from the continuous model are now given.

4.3.4 General results from the continuous model

Inductor and IS volume relation

By differentiating VOL_{TOT} from Eq. 4-30 with respect to λ_r

$$\frac{dVOL_{TOT}}{d\lambda_r} = \alpha^{3/5} \left(-\frac{3}{5} \lambda_r^{-8/5} + \frac{2}{5} \lambda_r^{-3/5} \right) \quad 4-31$$

and equating the result to zero, it is observed that a minimum or maximum occurs at $\lambda_r = 1.5$. The second derivative of Eq. 4-30 gives a positive value at $\lambda_r = 1.5$ (assuming $\alpha > 0$), which indicates that a volume minimum occurs when $IS_{VOL} = 1.5 \times L_{VOL}$ independent of all the other factors. This result is also obtained in [10].

L_{ESR} and IS_{ESR} relation

Rewriting Eq. 4-30 with k_Ω as the subject gives

$$VOL_{TOT} = \left(\frac{(k_\Omega + 1)^2}{k_\Omega} \right)^{3/5} f(E_{STORED}, s_{BP}, \rho_{metal}, t_{CH}, t_{Const}, \lambda_r), \quad 4-32$$

where the f designates some function derived from Eqs 4-28 and 4-30 that does not include k_Ω as an element. Differentiating Eq. 4-30 and equating the result to zero achieves a volume minimum or maximum at

$$k_\Omega = 1. \quad 4-33$$

The second derivative of Eq. 4-30 gives a positive value at $k_\Omega = 1$, which indicates that a volume minimum occurs at $k_\Omega = 1$ independent of the other parameters (assuming $\alpha > 0$). Thus a volume minimum occurs when the front-end is power-matched. This result is assumed in [10] but is formally proven here.

General observations

A volume minimum occurs at $E_{STORED} \rightarrow 0$, $\rho_{metal} \rightarrow 0$, $t_{Const} \rightarrow 0$ and $t_{CH} \rightarrow \infty$ and $s_{BP} \rightarrow \infty$ independent of one another and of the other parameters.

4.4 Discrete volume model

4.4.1 Shortcomings of the continuous model

There are two disadvantages posed by the continuous model.

Firstly, the continuous nature of s_{BP} in the continuous design algorithm may result in implementation problems in a practical system as system particulars such as inductor or IS configurations are not taken into account (along with their practical implications). These effects are demonstrated in Chapter 6. It is possible to determine these parameters from the continuous model but only as a post-optimisation calculation.

Secondly, and more importantly, is the effect of the switch on-state voltage on the design process. It is shown in 5.2.1 that the switch unit volume does not influence the volume optimisation process and that system modularity does not affect either the inductor, IS or switch volume. However, the switch on-state voltage Q_{V_ON} does play a role on the system volume. In order to incorporate this effect into the continuous model, Eq. 4-25 requires an alteration. Rewritten as

$$E_{STORED} = \left(\frac{IS_V - Q_{V_ON}}{L_{ESR} + IS_{ESR}} \left(1 - \exp\left(-\frac{t_{CH}}{t_{Const}}\right) \right) \right)^2 \frac{L}{2} \quad 4-34$$

according to Fig. 4-6, where Q_{V_ON} represents the total switch on-state voltage.

It is observed that decomposition of this equation to a form equivalent to Eq. 4-30 is not practical, as squaring of the circuit voltage will introduce additional energy terms that contain IS_V .

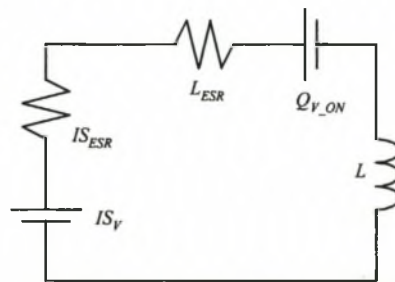


Fig. 4-6 Front-end circuit equivalent with Q_{V_ON}

4.4.2 Discrete model overview

Research in this project resulted in the development of a discrete model that addresses these shortcomings. The discrete model simply calculates the full system volume using the IS configuration (described by IS_{ESR} , IS_V , IS_I and IS_{VOL}) as the subject and calculates a matching inductor (using [73] p. 90f) for a spread of IS configurations. In this way it is possible to define some IS -inductor relation or optimisation procedure

objective other than that required by the continuous model. This is described where relevant. Also, the discrete model allows the incorporation of parameters such as the discrete nature of the IS and the effect of Q_{V_ON} . The effects of incorporating Q_{V_ON} into the design process are discussed in section 5.4. The following section provides a step-by-step analysis of both the continuous and discrete volume models.

4.5 Optimisation protocol

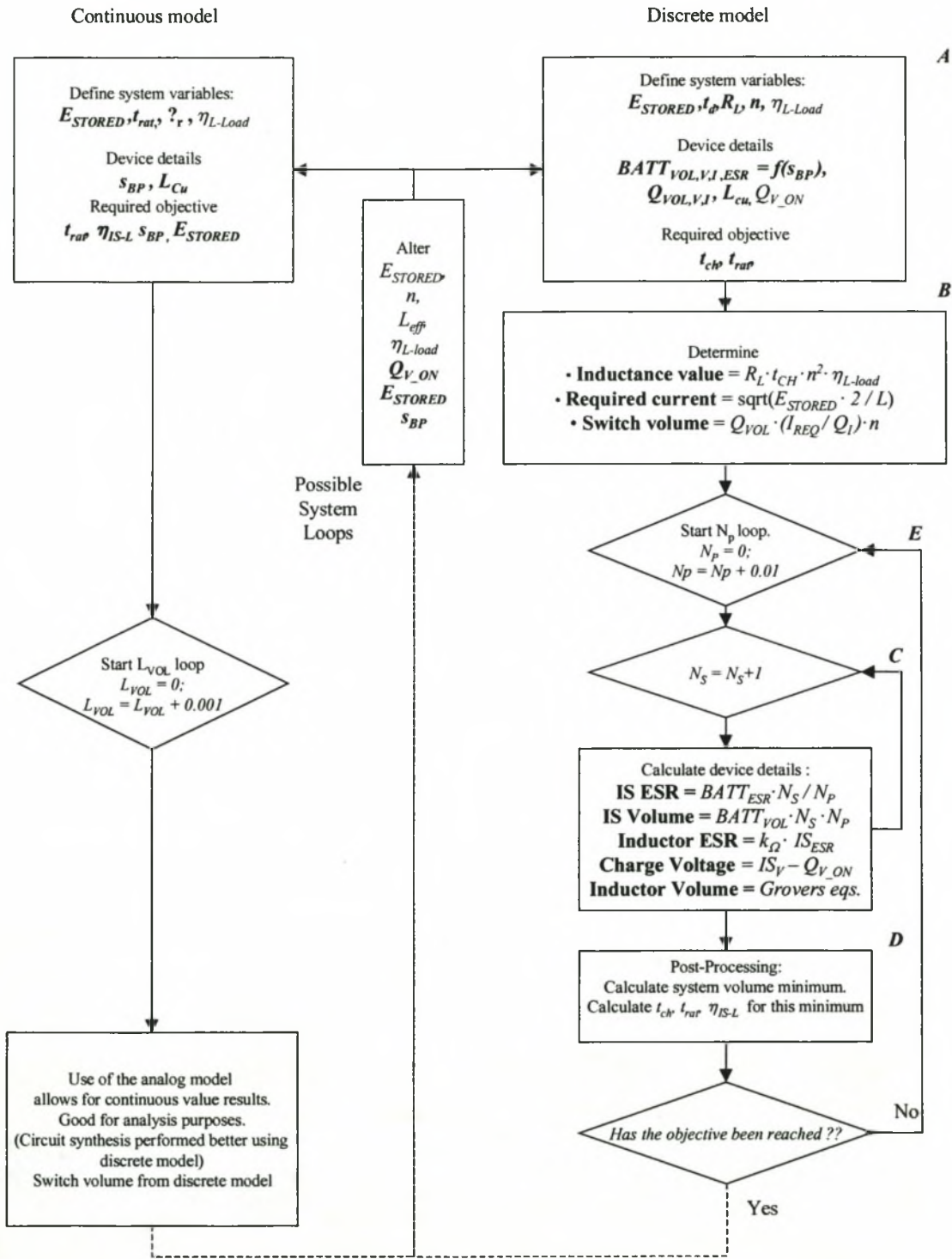


Fig. 4-7 Optimisation protocol

4.5.1 Continuous model implementation

The left-hand side of Fig. 4-7 shows the implementation of the continuous model. This model incorporates the description of section 4.3. Appendix H gives the main code describing the continuous model.

The system variables available in the continuous model are the required energy, E_{STORED} , subsystem volume ratio λ_r (usually set to 1.5) and charge time ratio, $t_{rat} \cdot \eta_{L-load}$ can also be used as a multiplicative energy modifier to compensate for back-end transfer losses.

The device variables available to the designer are battery power density s_{BP} and inductor material (usually copper or aluminium).

The designer defines the optimisation objectives. Ref. [10] uses t_{rat} as the iteration subject to obtain a required η_{IS-L} , for example. Chapter 5 uses the continuous model for a number of simulations.

The method employed in this project is to define the optimisation objective – for example, to examine the effect of E_{STORED} on η_{IS-L} – and calculate the system volume (using L_{VOL} as the iteration subject) for range of values of E_{STORED} . The minimum for each E_{STORED} is determined, η_{IS-L} for each system at those minima is further calculated and the results are processed.

4.5.2 Discrete model implementation

This model incorporates a robust optimisation protocol where all the possible system constructions are considered and the optimum system is simply read from the data.

Some assumptions are made according to the generalised results discussed in section 4.3.4. For all system calculations performed using the discrete model, it is observed that the ratio λ_r always equals 1.5 at the minimum, no matter what the design objective. This result is not proven formally for all optimisation conditions.

Block A of Fig. 4-7 defines all the pre-optimisation parameters.

The system variables required from the designer are the stored energy E_{STORED} , back-end discharge time t_d , load approximation R_L , module number n and expected back-end discharge efficiency, η_{L-load} , which can be used as a stored-energy

modifier. η_{L-load} is defined beforehand as it incorporates a number of considerations that cannot be included in the optimisation protocol.

The required device details include all of the battery unit details (which can be derived from s_{BP} and one battery unit detail, typically the open circuit voltage $BATT_V$) and the switch unit details.

Lastly, the required design objective is defined. Due to the fact that so many variables play a role in calculating the system volume, it is up to the designer to isolate the relevant aspects and perform system studies on these alone. The desired results are of course the resultant system volume and system efficiency (in this case the front-end efficiency, considered separately from the back-end efficiency). The relevant optimisation objectives used in this research include the effect of the charge time t_{CH} and the charge time ratio t_{rat} on system volume and efficiency.

Block B of Fig. 4-7 calculates parameters used as constants in the optimisation procedure. These are the required full inductance value L_{ST} , required charge current I_{REQ} and the total switch volume (which is independent of the optimisation procedure). These parameters are discussed in the relevant section.

Block C of Fig. 4-7 incorporates the inner loop of the main optimisation procedure. This loop calculates sub-system volumes for a sweep of series IS increments, N_S , where the parallel width N_P is defined by the outer loop. The IS volume is simply a multiplication of the battery unit volume by the series and parallel unit number (either discrete or continuous). The resultant available charge voltage is calculated from IS_V and Q_{V_ON} . The inductor volume is calculated from the discrete model described in 4.2.3 using a known L_{ST} (calculated above) and an L_{ESR} calculated from some relation to IS_{ESR} . Fig. 4-7 shows the inductor ESR being equated to the IS ESR with a modifier. Although section 4.3.4 shows that a value of $k_{\Omega} = 1$ results in an optimum volume, it is possible that a non-continuous s_{BP} would result in a different optimum. In this case Eq. 4-25 would be subject to certain restrictions on IS_V and IS_{ESR} , which would result in some additional coupling of these variables to the ESR modifier k_{Ω} that could require a different k_{Ω} value.

The prototype constructed in this project is such a case and the ramifications are discussed in 5.1.

Block D of Fig. 4-7 processes the results according to the design objective. If the objective has been reached, the optimisation is terminated.

Block E incorporates the outer loop and uses increments of N_p , either discrete or continuous.

4.5.3 Possible system loops

This block groups the system parameters that do not have minima but which are also of interest to the designer. Depending on which parameter is of interest, either the continuous model or discrete model can be used. The parameter L_{eff} can be used as an inductor volume modifier to incorporate the effect of isolation thickness, for example.

4.5.4 Block A and back-end efficiency η_{L-Load}

Block A is composed of the user-defined parameters and user defined objectives. All are system specific or technology specific and invariant to the result of the optimisation procedure, except for the back-end transfer efficiency η_{L-Load} . This factor is dependent on a number of factors and is dealt with separately and independently of the optimisation procedure. It can be used as value modifier in block B of the optimisation procedure.

Five energy components are represented with this factor, described below. It can be written either as a proportional inductance modifier or used as an energy addition term.

DC transfer efficiency

The DC transfer efficiency is simply a ratio of the energy dissipated in the load over the total stored energy. As the final discharge sequence must be variable, the two extreme sequence considerations of full parallel discharge state and full series discharge state are defined. The total energy stored in the coil is given as

$$E_{STORED} = \frac{I_{REQ}^2 L_{ST}}{2} . \quad 4-35$$

The back-end time constant (used as the minimum discharge time, or full parallel discharge state) is reproduced here from Eq. 4-52 as

$$t_d = \frac{L_{ST}}{\left(R_L + \frac{L_{ESR_TOT}}{n^2} \right) n^2} . \quad 4-36$$

The energy dissipated in the load during the full discharge cycle is

$$\begin{aligned}
 E_{LOAD_PAR} &= R_L \int_0^{\infty} (nI_{REQ})^2 \exp\left(\frac{-2t}{L_{ST}/(n^2(R_L + L_{ESR_TOT}/n^2))}\right) dt \\
 &= \frac{I_{REQ}^2 L_{ST}}{2} \frac{R_L}{R_L + \frac{L_{ESR_TOT}}{n^2}}
 \end{aligned} \tag{4-37}$$

Substitution of Eqs 4-35 and 4-37 into 4-38 into

$$\eta_{L-R} = \frac{E_{STORED} - E_{LOST}}{E_{STORED}} = \frac{E_{LOAD_PAR}}{E_{STORED}}, \tag{4-38}$$

gives the parallel discharge back-end transfer efficiency as

$$\eta_{DC_PAR} = \frac{R_{LOAD}}{R_{LOAD} + \frac{L_{ESR_TOT}}{n^2}}. \tag{4-39}$$

For the series state, the back-end transfer efficiency is simply

$$\eta_{DC_SER} = \frac{R_{LOAD}}{R_{LOAD} + L_{ESR_TOT}}. \tag{4-40}$$

This efficiency can be taken into account by defining minimum allowable transfer efficiency and making sure that, as part of the algorithm post-calculations or additional outer-loop, it is not exceeded. Depending on the type of switch sequence used, the two efficiency limits can be used as references. For this system, η_{DC_PAR} is used. It appears that the DC efficiency is not a problem with volume-optimised systems.

Skin effect losses

For skin effect considerations, the skin depth for a 1 kHz signal is 2.4 mm ([74] p. 748). Assuming a quarter flank of a sine wave to approximate an exponential discharge, this corresponds to a discharge time of 250µs. Assuming that this ms pulse supply delivers pulses over the 1ms time span, it is assumed that no skin effect considerations need to be taken into account. This can be verified in the post-process calculations by comparison of the conductor diameter to the skin depth.

Unrecoverable energy due to eddy losses

Ref. [9] gives a detailed discussion on the influence of the inductor geometry on this transfer efficiency. Analogous to skin effect, yet independent of it, sudden collapse of

the storage field may result in coupling of the field to the actual conductors. This is particularly a problem in single-winding planar PCC-type coils, where the relaxed storage field is orthogonal to the conductor plane, and according to [9], could result in a back-end transfer efficiency of less than 80%. For multi-winding coil geometries (as proposed in this project) this does not appear to be a problem, however.

Load utilisation of the energy

Ref. [4] discusses the transfer of energy from the inductor to the load with the concept of usable energy in mind.

Switching losses

Ref. [10] considers switching losses and discusses limit parameters for the allowable losses. Consideration of this parameter is handled slightly differently in this project as the switches implemented – namely, solid-state switches – switch fast enough for the assumption that the storage inductor current remains constant. The full circuit description is given in Chapter 3. The full switch transient is discussed in section 3.5.

For worst-case switching we assume that the transient is wholly inductive, there is no snubber capacitor and that the device voltage has to reach full voltage before current can drop. The energy

$$E_{OFF} = \frac{I_0 V_0 t_{OFF}}{2}, \quad 4-41$$

is the worst-case turn-off energy, where I_0 is the conduction current at turn-off, V_0 the commutation voltage and t_{OFF} the device turn-off time shown in Fig. 4-8.

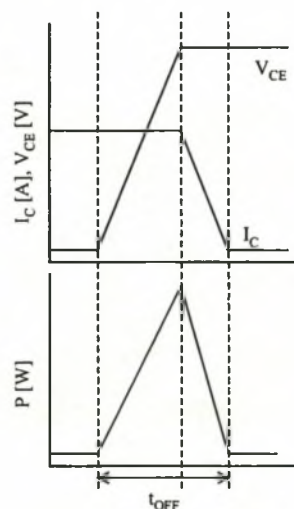


Fig. 4-8 Worst-case IGBT turn-off approximation

Assuming a current of 40 kA and a load voltage of 20 kV, we get a 400 J/ μ s switching. Thus for even a GTO of slow switching time (30 μ s), the switching energy is 12 kJ, just over 2% of the load energy. As HVIGBTs switch in under 2 μ s, it is assumed that the switching energy is negligible.

The prototype utilises large snubber capacitors across its devices and the switches effectively soft-switch. Eq. 4-41 is the total switching losses for the worst-case scenario.

All of these considerations are mentioned here but are assumed not to alter the discharge energy; $\eta_{L-Load} = 1$. Exact determination of this factor and inclusion into the optimisation procedure during optimisation is difficult; however, its inclusion in the as a post- or pre-processed parameter is trivial. The modifier can be appended to the current value (increasing current value) or the inductor value; either is sufficient.

4.5.5 Block B and calculated non-changeable parameters

$$\text{Inductance value} = R_L t_d n^2 \eta_{L-Load}$$

The required inductance value of the whole inductor (in full series connection) is L_{ST} . This design assumption is important and very subjective; it is assumed in this design that the output pulse must have a variable discharge length (but with a constant discharge energy).

The minimum discharge time is used as the reference.

For a modular supply, the shortest discharge time is obtained when all the inductors are discharged in parallel into the load. If the load approximation as a resistance is made, the minimum discharge time is defined as a single discharge time constant between the load and the storage element in full parallel discharge configuration. As discussed in section 4.2.4, we assume that the modules in the inductor are balanced. This means that for each module $L_{ESR} = L_{ESR_TOT} / n$, $L_{ESR1} = L_{ESR2} = \dots = L_{ESRp} = \dots = L_{ESRn}$ and $i_1 = i_2 = \dots = i_p = \dots = i_n$ in Fig. 4-9, where n is the total module number.

The diodes are included in Fig. 4-9 to indicate that there is no electrical energy transfer between modules. It is clear that the branch voltages are related to one another and the load by

$$-v_{load} = v_1 + v_{ESR1} = v_2 + v_{ESR2} = \dots = v_p + v_{ESRp} = \dots = v_n + v_{ESRn} . \quad 4-42$$

Using a generic inductor L_p

$$-v_{load} = -R_L \cdot \sum_{q=1}^n i_q = M_{1p} \frac{di_1}{dt} + M_{2p} \frac{di_2}{dt} + \dots + L_p \frac{di_p}{dt} + \dots + M_{np} \frac{di_n}{dt} + i_p L_{ESRp} , \quad 4-43$$

describes Eq. 4-42 for v_p . The modules are coupled to every other module with an average coupling factor k_c that is homogenous throughout the system.

By substitution of $M_{qp} = k_c L_p$ for $q = 1..n, q \neq p$. Eq. 4-43 is rewritten as (where the currents are all equal)

$$\begin{aligned} -R_L \sum_{q=1}^n i_q - i_p L_{ESRp} &= -i_p \cdot (nR_L + L_{ESRp}) \\ &= k_c \cdot L_p \frac{di_1}{dt} + k_c \cdot L_p \frac{di_2}{dt} + \dots + L_p \frac{di_p}{dt} + \dots + k_c \cdot L_p \frac{di_n}{dt} , \\ &= L_p (1 + (n-1)k_c) \frac{di_p}{dt} \end{aligned} \quad 4-44$$

which translates to

$$i_p = - \frac{L_p (1 + (n-1)k_c)}{(nR_L + L_{ESRp})} \cdot \frac{di_p}{dt} . \quad 4-45$$

The discharge time constant is calculated from Eq. 4-45 as

$$t_d = \frac{L_p (1 + (n-1)k_c)}{(nR_L + L_{ESRp})} , \quad 4-46$$

and as a result the individual module self-inductance can be calculated as

$$L_p = \frac{t_d \cdot (nR_L + L_{ESRp})}{(1 + (n-1)k_p)} . \quad 4-47$$

Eq. 4-47 calculates the self-inductance of an individual module in an n-module system that allows for a required discharge time in full parallel discharge configuration. It is in the designer's interest to determine the value of the whole inductor when all the modules are connected in series, or the value of L_{ST} , as it is this value that is used in the optimisation procedure.

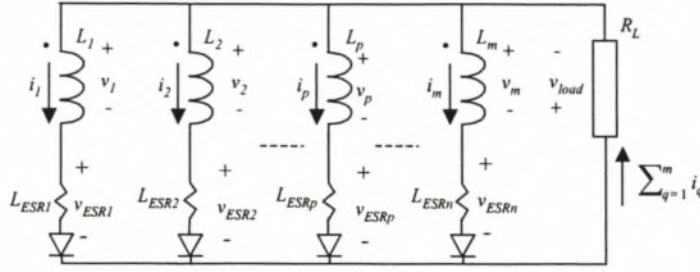


Fig. 4-9 Parallel discharge equivalent

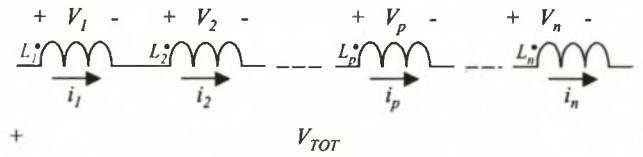


Fig. 4-10 Series inductor equivalent

For this calculation, it is not necessary to incorporate the inductor ESRs as it is simply the full inductance that is required. It is clear from Fig. 4-10 that $i_1 = i_2 = \dots = i_p = \dots = i_n$. Also, if $L_1 = L_2 = \dots = L_p = \dots = L_n$ and k_c is homogenous throughout, then $v_1 = v_2 = \dots = v_p = \dots = v_n$. For a module L_p its voltage v_p is described by

$$\begin{aligned} v_p &= M_{1p} \frac{di_1}{dt} + M_{2p} \frac{di_2}{dt} + \dots + L_p \frac{di_p}{dt} + \dots + M_{np} \frac{di_n}{dt} \\ &= k_c \cdot L_p \frac{di_1}{dt} + k_c \cdot L_p \frac{di_2}{dt} + \dots + L_p \frac{di_p}{dt} + \dots + k_c \cdot L_p \frac{di_p}{dt} \\ &= L_p (1 + (n-1)k_c) \frac{di_p}{dt} \end{aligned} \quad 4-48$$

Also, $v_{TOT} = v_1 + v_2 + \dots + v_p + \dots + v_n = n \cdot v_p$ and as a result

$$v_{TOT} = L_p n (1 + (n-1)k_c) \frac{di_p}{dt}, \quad 4-49$$

and the total series inductance

$$L_{ST} = L_p n (1 + (n-1)k_c), \quad 4-50$$

can be calculated. Substitution of L_p of Eq. 4-47 into the above equation gives

$$\begin{aligned} L_{ST} &= (nR_L + L_{ESRp}) \cdot t_d n \\ &= \left(R_L + \frac{L_{ESR_TOT}}{n^2} \right) \cdot t_d n^2, \end{aligned} \quad 4-51$$

where the resultant time constant for full parallel discharge can be calculated as

$$t_d = \frac{\frac{L_{ST}}{n^2}}{R_L + \frac{L_{ESR_TOT}}{n^2}}. \quad 4-52$$

As a result it is clear that the effective total required inductance is independent of the mutual coupling but dependent on the module count. Thus, while the total required inductance remains constant, its modules alter in self and mutual inductance value, dependent on the coupling factor, to match both the total inductance and correct discharge time.

It is also clear that the L_{ESR_TOT} plays a role in the discharge time. However, L_{ESR_TOT} is used in the optimisation procedure; incorporation of L_{ESR_TOT} would be cumbersome. As a result, an assumption is made that L_{ESR_TOT} is negligible in this calculation. To keep this assumption general, a maximum value is set; if L_{ESR_TOT} exceeds this value, the calculation is tagged. In actual calculation with typical system values, this situation does not occur. The required inductance value is thus approximated as

$$L_{ST} = R_L t_d n^2. \quad 4-53$$

η_{L_Load} can be included at this stage as a multiplacative modifier; this research, however, considers $\eta_{L_Load} = 1$. This equation is central to the volume model being independent of module count.

This form of system description – the recognition of the L_p and k_c – can also be used in the development of the inductance matrix \mathbf{M}_n of section 4.2.4.

The continuous model of section 4.3 requires a constant τ_l for an optimised system; thus the inductor volume is assumed independent of the actual inductor value, so long as its τ_l remains constant (thus the IS would reconfigure, yet retain its constant volume, to accommodate the resultant change in L_{ESR_TOT}). This would imply the unlikely situation that the inductor value can be tailored to result in any discharge time t_d for any load; however, this is impossible as the inductor stores a defined energy. This quandary is not considered in the continuous model but it is evident here that the smaller the load or the longer the charge time, the more the energy that is dissipated in the inductor itself. Thus the back-end discharge efficiency acts to limit the possible discharge times.

$$\text{Required current} = \sqrt{\frac{2 \cdot E_{\text{STORED}}}{L_{\text{ST}}}}$$

This is the standard inductor equation; the required current is referred to as I_{REQ} .

$$\text{Switch Volume} = Q_{\text{VOL}} \cdot n \cdot \frac{I_{\text{REQ}}}{Q_I}$$

Each switch is rated at the load voltage.

The required switch volume is a linear relation dependent on the required current and unit volume alone. For a required inductor value of $L_{\text{ST}} = R_L t_d n^2$ and a total stored energy of $E_{\text{STORED}} = \frac{1}{2} L_{\text{ST}} I_{\text{REQ}}^2$, the equation

$$\sqrt{\frac{2E_{\text{STORED}}}{R_L t_d}} = n I_{\text{REQ}}, \quad 4-54$$

is calculated. Thus it is clear that there is a linear (inverse) relationship between the module number and the current. Also, the full switch volume becomes independent of the module number because it is highly modular. Thus for a set required energy, load resistance and discharge time, the total required switch volume is

$$\sqrt{\frac{2E_{\text{STORED}}}{R_L t_d}} \cdot \frac{Q_{\text{VOL}}}{Q_I}, \quad 4-55$$

which is independent of module number.

4.5.6 Block C and final volume calculations (discrete model)

Calculation of the system volume for all possible IS configurations is performed here.

The assumption of a matched IS and inductor made (validated by section 4.3.4). The IS voltage available for the charging of the inductor is calculated by simply subtracting the full Q_{V_ON} (from all the serialised switches and modules connected in series at this stage) from the IS voltage IS_V . For correlation with the continuous model, Q_{V_ON} is equated to zero.

4.5.7 Final volume calculations (continuous model)

Eq. 4-29 is used. The inductor volume L_{VOL} is cycled through a range of volumes and the IS volume is calculated to match; a volume minimum is easily achieved. A

number of assumptions need to be made for the calculation; values for t_{rat} , λ_r and k_Ω are assumed before the calculation (correlation with the discrete model uses these factors as optimisation objectives).

4.5.8 Optimisation objective s = t_{CH} , t_{rat} , η_{IS_L}

The three main considerations that are required are:

1. Is there sufficient heat exchange within the system to ensure that no sub-system critical temperatures are exceeded?
2. Does the front-end transfer efficiency η_{IS_L} match shot repetition or storage specifications?
3. Is the charge time within system specifications?

Device critical temperatures

Critical temperatures of the sub-systems are very device specific. The IS has a temperature-dependent ESR and energy storage capability. Energy dissipated in the battery alters its characteristics; this factor is highly technology dependent and is not considered further.

The inductors temperature may be a concern if construction methods result in very high thermal impedance between the conductors and ambient levels. To quantify the temperature rise, the worst case of no heat exchange during the charge cycle is assumed. The temperature rise of any material is given in [77] as

$$\Delta T = \frac{Q}{mc}, \quad 4-56$$

where ΔT is the change in temperature, Q the injected energy, m the total material mass and c the specific heat constant of the material. At 25°C c is 387 J/kg°C for copper. The temperature rise is calculated as

$$\begin{aligned} \Delta T &= \frac{Q}{mc} = \frac{I_{req}^2 t_{CH} L_{ESR_TOT}}{L_{cond_length} \cdot \delta \cdot den_{Cu} \cdot c} = \frac{I_{req}^2 t_{CH} \cdot \rho_{Cu} \cdot \delta / L_{cond_length}}{L_{cond_length} \cdot \delta \cdot den_{Cu} \cdot c} \\ &= \frac{I_{req}^2 t_{CH}}{L_{cond_length}^2} \cdot \frac{\rho_{Cu}}{den_{Cu} \cdot c}, \end{aligned} \quad 4-57$$

where I_0 is the charge current, t_{CH} is the charge time, ρ_{Cu} copper resistivity at 25°C, den_{Cu} copper density at 25°C. L_{cond_length} is the length of the conductor used to make the inductor and δ is the conductor diameter.

The injected energy is taken as the worst-case DC supply waveform for the full charge time. It is observed that for copper coils required for minimum volume 0.5MJ systems, the temperature rise per shot is approximately 6°C. Sufficient heat exchange is required to manage this extra heat. However, this project does not take this factor into account.

Temperature management of the switches is a different matter. This is dealt with in section 3.10.

Front-end transfer efficiency η_{IS_L}

The front-end transfer efficiency η_{IS_L} is dependent on the charge time and the charge cycle waveform. For a long-charge cycle, where the charge time is a number of front-end time constants, this efficiency is obviously lower.

It assumed that all the energy stored in the inductor at the firing time is transferred to the load ($\eta_{L-load} = 1$). Therefore the transferred energy, or the load energy E_{load} , is equal to the stored energy E_{STORED} or $\frac{1}{2}L_{ST}I_{REQ}^2$, while the total used energy is equal to the transferred energy plus the energy dissipated in the device ESRs and the switches, or $E_{DISSIPATED}$, during the charge cycle.

The front-end transfer efficiency equation is thus equal to

$$\eta_{IS-L} = \frac{E_{STORED}}{E_{STORED} + E_{DISSIPATED}}, \quad 4-58$$

where

$$E_{DISSIPATED} = E_{BATT_ESR} + E_{L_ESR} + E_{SWITCH_CONDUCTION} \quad 4-59$$

The switches' switching losses are considered as part of the back-end transfer efficiency. The resistive losses are

$$\begin{aligned} E_{BATT_ESR} + E_{L_ESR} &= \int_{t=0}^{t_{CH}} R_T \left[I_{final} \left(1 - e^{-\frac{t}{t_{Const}}} \right) \right]^2 dt \\ &= R_T I_{final}^2 t_{Const} \left(\frac{t_{CH}}{t_{Const}} + 2e^{-\frac{t_{CH}}{t_{Const}}} - \frac{1}{2}e^{-2\frac{t_{CH}}{t_{Const}}} - \frac{3}{2} \right), \\ &= \frac{I_{final}^2 L_{ST}}{2} \cdot \left(4e^{-\frac{t_{CH}}{t_{Const}}} + 2\frac{t_{CH}}{t_{Const}} - e^{-2\frac{t_{CH}}{t_{Const}}} - 3 \right) \end{aligned} \quad 4-60$$

where

$$t_{Const} = \frac{L_{ST}}{R_T}, \quad 4-61$$

and $R_T = IS_{ESR} + L_{ESR_TOT}$.

The switches' conduction losses are given as

$$\begin{aligned} E_{SWITCH_CONDUCTION} &= \int_{t=0}^{t_{CH}} nQ_{V_ON} I_{final} \left(1 - e^{-\frac{t}{t_{Const}}} \right) dt \\ &= nI_{final} Q_{V_{on}} t_{Const} \left(e^{-\frac{t_{CH}}{t_{Const}}} + \frac{t_{CH}}{t_{Const}} - 1 \right), \end{aligned} \quad 4-62$$

where I_{final} is equal to the charge current when $t \rightarrow \infty$, and Q_{V_ON} in this case is the on-state voltage of each module turn-on switch. If the charge time ratio $t_{rat} = \frac{t_{CH}}{t_{Const}}$ is known where

$$I_{REQ} = I_{final} (1 - e^{-t_{rat}}), \quad 4-63$$

Then the conduction can thus be calculated as

$$E_{SWITCH_CONDUCTION} = \frac{nI_{REQ} \cdot Q_{V_ON} \cdot t_{CH}}{1 - e^{-t_{rat}}} \left(1 - \frac{1 - e^{-t_{rat}}}{t_{rat}} \right), \quad 4-64$$

and the resistive losses as

$$E_{BATT_ESR} + E_{L_ESR} = \frac{L_{ST} I_{REQ}^2}{2} \frac{(4e^{-t_{rat}} + 2t_{rat} - e^{-2t_{rat}} - 3)}{(1 - e^{-t_{rat}})^2}. \quad 4-65$$

Further elaboration of this is performed in the next chapter.

Charge times t_{CH} and t_{rat}

The charge time ratio is used by Soreq [10] as a system constant used to compare system considerations (such as volume and efficiency) because the continuous model lends itself well to the use of t_{rat} . For correlation purposes with [10], this system dependence analysis is discussed in section 5.7. For other system concerns exterior to the technical concerns of the system itself (such as fire-ready time), t_{CH} is important; its analysis is included in section 5.8.

4.6 Summary

This chapter introduces the inductive storage PFN as a system composed of sub-systems. These sub-systems are identified and each one is modelled using parameters

applicable to a volume-optimisation process. The inter-subsystem relationships are modelled as functions of these parameters.

An analytical model (continuous model) is described. Some general system results are discussed. The analytical model has a few shortcomings; these are identified.

An alternative model – the discrete model – that allows for the circumvention of these shortcomings is presented and discussed.

The full optimisation process, including the initially required parameters, calculable parameters, iteration parameters and possible optimisation objectives, is presented and discussed. Lastly, some additional outer-loop considerations (used for further system analysis) are identified.

CHAPTER 5

VOLUME OPTIMISATION RESULTS

5.1 Introduction

This chapter documents the results of the design algorithms developed in the preceding chapter.

This section compares the model results to one already published, that of Soreq [12], identifies model differences, clarifies what the designer can determine from the models and discusses the assumptions made in the design process.

The following sections discuss the various parameters available to the designer and consider the influence(s) of these parameters on the system volume. As these parameters are numerous, each one is considered independently of the other. This approach necessitates certain assumptions which are given at the start of each discussion.

Lastly a suggestion for a 500 kJ system is made. The full system (with no packing-factor modifier) is less than 1 m³ using contemporary device technologies. The figures included in this chapter are marked with a small circle; this marker indicates where on that particular graph the 500 kJ system suggestion falls.

5.1.1 Model Correlation

Soreq [10] focuses on the design of a single-stage inductive storage PFN using the continuous model of the previous chapter and utilising non-solid state switches. The system is specified at 500 kJ; this energy level is correspondingly assumed for comparative purposes in Table 5-1.

Table 5-1 Model discrepancies

	<i>Soreq</i>	<i>Grover₁</i>	<i>Grover₂</i>	<i>Grover₃</i>
Factor K of Eq. 4-11	6.03×10^{-8}	3.76×10^{-8}	3.95×10^{-8}	<i>na</i>
IS _{VOL} +L _{VOL} (m ³)	0.28	0.37	0.36	0.36

It is important to note that there are a few differences (none radical) between the model developed in Ref. [10] and the model used here. The constant of Eq. 4-11 differs; this results in optimisation values that are different by up to 20%. Also, the definition of battery power density in this paper differs from that of [10]; this has been discussed and is not repeated here. Table 5-1 is developed with the assumption that $\lambda = 1.5$, $s_{bp} = 80 \text{ kW/l}$, $t_{RAT} = 1.5$, $E_{STORED} = 500 \text{ kJ}$, $Q_{V_ON} = 0$, a matched front-end and an aluminium inductor. The Soreq result documented in [10] corresponds to that calculated here using Soreq's factor value in the continuous model. Grover₁ is taken directly from [73]; Grover₂ is calculated from Eq. 4-11 and Grover₃ is calculated using the discrete model discussed in section 4.4 and assuming Q_{V_ON} is zero. Calculations using the method proposed in Appendix G indicates that a value closer to 4×10^{-8} is correct. Grover₂ is further assumed to be the most accurate value. The influence of Q_{V_ON} is not incorporated into the Soreq model or the results documented in Table 5-1.

5.1.2 What information can be obtained from the model?

The aims of this project are to determine the feasibility of developing a modular, inductive storage millisecond PFN capable of delivering 500 kJ in the required time span to an ETC load; the whole system including the inductor, IS and switch gear should have a volume of less than 1 m^3 . A number of considerations play off against one another.

These can be listed as follows:

1. Is the delivered pulse shape and pulse energy a sufficient match (dealt with in chapter 3)?
2. At what system conditions does the system volume minimum occur?
3. What is the effect of system modularity?
4. Is the system thermally stable?
5. Does the system efficiency match specifications?
6. Is the system electrically stable (dealt with in 5.1)?

Points 2 to 5 are considered in this chapter.

5.1.3 Assumptions

A number of pre-design assumptions are made here. These are:

1. The inductor is a single Brooks coil structure and is made of copper, unless otherwise stated. Isolation considerations are not taken into account.
2. The volume values documented exclude the switch volume unless otherwise stated.
3. The battery power density is assumed to be 80 kW/l (or 20 kW/l by Soreq's definition), unless otherwise stated. For a matched load, the battery will deliver half its short-circuit current capability to the load and at a voltage level of half the battery open-circuit voltage. Thus numerical value of s_{BP} used in these designs is 4 times that used by Soreq for the same battery technology.
4. The charge ratio t_{rat} is assumed to be 1.5 (arbitrarily), unless otherwise stated.
5. The IS and inductor are power matched as according to section 4.3.4, unless otherwise stated.
6. $\lambda_r = 1.5$ as according to section 4.3.4, unless otherwise stated.

5.2 Dependence of volume and η_{IS-L} on module number

The sub-system volumes are not affected by modularity number, assuming the sub-systems themselves are sufficiently modular. Each sub-systems configuration is, however, changed, depending on the total module number required. For instance, increasing the module number results in an increased inductance value L_{ST} . However, it is observed that the required inductance L_{ESR_TOT} is also altered to compensate exactly so that the full inductor volume remains constant. Likewise, a higher inductance requires a higher voltage IS_v yet requires a lower IS_l ; full IS volume remains constant but the IS is simply reconfigured. This is described in the following sections.

5.2.1 Switch volume and η_{IS-L} dependence on modularity number

Eq. 4-55 (total switch volume), repeated here as

$$Q_{VOL_TOT} = \sqrt{\frac{2E_{STORED}}{R_L \tau_d}} \cdot \frac{Q_{VOL}}{Q_I}, \quad 5-1$$

shows that the switch volume is independent of the system modularity assuming that the devices themselves are sufficiently modular. Typical system ratings of 20 kV and 40 to 80 kA will require a great deal of switch serialisation and paralleling using

contemporary device technologies (refer to section 5.9). Thus for a set energy requirement, the full switch volume is divided by the number of modules used to determine the switch volume per module.

If the switch volume is independent of the modularity number, it follows that the switches all need to conduct the same current and hold the same voltage, independent of actual configuration. It follows therefore that the system efficiency dependence on modularity as far as the switches are concerned is also independent of the level of modularity incorporated.

5.2.2 Inductor and battery volume dependence on modularity

Inductor and battery volume necessarily need be considered together as they are interdependent. The required IS volume can be calculated by

$$IS_{VOL} = \frac{S_{BP}}{S_{BP}} = \frac{IS_V^2}{IS_{ESR} \cdot S_{BP}} = \frac{(I_{final} \cdot (L_{ESR_TOT} + IS_{ESR}))^2}{IS_{ESR} \cdot S_{BP}}, \quad 5-2$$

where I_{FINAL} is the current that will flow in the circuit at $t \rightarrow \infty$. Assuming front-end matching, this can be simplified to

$$IS_{VOL} = \frac{4I_{final}^2 L_{ESR}}{S_{BP}}. \quad 5-3$$

The required current is calculated is

$$I_{REQ} = \sqrt{\frac{E_{STORED}}{R_{LOAD} \tau_d}} \cdot \frac{1}{n} = \frac{const}{n}, \quad 5-4$$

where *const* is used here (and further on) to represent variables that are not relevant to the calculation. The required current is therefore related linearly to the final current by

$$I_{final} = \frac{I_{REQ}}{1 - e^{-t_{RAT}}} = \frac{const_2}{n}. \quad 5-5$$

Substitution of Eq. 5-5 into Eq. 5-3 gives

$$IS_{VOL} = \frac{4I_{final}^2 L_{ESR_TOT}}{S_{BP}} = \frac{4const_2^2 L_{ESR_TOT}}{n^2} = \frac{const_3 \cdot L_{ESR_TOT}}{n^2}. \quad 5-6$$

It is therefore clear that for the battery volume to remain constant independent of the module number, the inductor ESR (L_{ESR_TOT}) must be

$$L_{ESR_TOT} = \frac{IS_{VOL} \cdot n^2}{const_3} = const_4 \cdot n^2. \quad 5-7$$

It is further proved that for a balanced system, this is the case. Substituting

$$L_{ST} = R_{LOAD} t_d n^2 = const_5 \cdot n^2, \quad 5-8$$

and 5-7 into τ_i gives

$$\tau_i = \frac{L_{ST}}{L_{ESR_TOT}} = \frac{const_5 \cdot n^2}{const_4 \cdot n^2} = const., \quad 5-9$$

which shows that the system volume is independent of the module count.

As a result, both the inductor volume and the IS volume remain independent of the system modularity. This can be intuitively described with the understanding that it is only the inductor time constant τ_i that needs to remain unchanged; changing of the value of the inductor value requires proportional changing of the inductor ESR; this does not change the volume of the IS but only its configuration (series and parallel components adjust to match the front-end ESRs).

Peripheral hardware requirements – such as the bus-bar architecture or inter-module isolation – may alter this relation, but this is not brought into the optimisation protocol.

5.2.3 Back-end η_{L-load} dependence on modularity

Eqs. 4-39 and 4-40 show that for a defined system with n modules, the series discharge state results in a lower efficiency than the parallel discharge state; this can be intuitively seen as current flows longer in the series discharge state. However, the design protocol discussed in 3.1 aims at allowing for a defined discharge time t_d that is independent of the module number. Intuitively, we might expect the transfer efficiency to also remain independent of the module count. For a system with a defined E_{STORED} and discharge time t_d , a volume-optimised system requires L_{ESR_TOT} as a function of n (Eq. 5-7) to be equal to

$$L_{ESR_TOT} = L_{ESR_BASE} \cdot n^2, \quad 5-10$$

where L_{ESR_BASE} is L_{ESR_TOT} at $n = 1$. Substitution of Eq. 5-10 into Eq. 4-39 gives

$$\eta_{DC_PAR} = \frac{R_{LOAD}}{R_{LOAD} + L_{ESR_BASE}}, \quad 5-11$$

for all values of n . It is clear therefore that the discharge efficiency of a modular system remains relatively independent of the level of modularity.

5.3 Switch volume

Eq. 4-55 describes the relationship of the switch volume to the system specifications assuming that the modules are balanced. As is observed, the switch volume is independent of the IS and inductor configuration (there is a degree of dependence on the charge time t_{CH} as described in section 4.2.2 that is considered only as a post-processed parameter). Furthermore, section 5.2.1 shows that the switch volume is also independent of the module count used. It is possible therefore to calculate the required switch volume wholly independently of the module count and IS and inductor configurations. The effect of the on-state voltage Q_{V_ON} does need to be considered in the optimisation procedure; this is discussed in the following section.

5.4 Effect of Q_{V_ON} on system volume model

As discussed in section 4.4.1, if the switch on-state voltage Q_{V_ON} is included in the optimisation procedure, the continuous model is no longer valid (according to Fig. 4-6). The discrete model proposed does solve this problem. However, dependence on the discrete model for results implies that the generalised results discussed in section 4.3.4 are no longer valid. Furthermore, the exact value of Q_{V_ON} is very device specific. Despite this, however, it is observed with the use of the discrete model that the ratio $\lambda=1.5$ still holds independent of the magnitude of Q_{V_ON} v (although this is not proven formally).

No formal proof of the coupled effect of the system modularity and Q_{V_ON} on the system volume is provided here. It is observed, however – with the use of the discrete model – that, while the volume of the system itself is affected by a non-zero Q_{V_ON} , the effect is independent of the module number used. This can be interpreted intuitively; it is observed that the required current I_{req} is inversely proportional to the module number in the relation as defined in Eq. 4-54. For zero Q_{V_ON} the IS volume remains independent of module count; the full IS volume is proportional to

$$IS_{VOL} \propto N_P N_S, \quad 5-12$$

where N_P is the number of parallel units (corresponding linearly to I_{REQ}) and N_S is the number of series units compromising the full IS volume. This implies a linearly

proportional relationship between IS_V (voltage) and the module count. It is clear that Q_{V_ON} is linearly proportional to the module number in the relation

$$Q_{V_ON}(n) = Q_{V_ON}(1) \cdot n. \quad 5-13$$

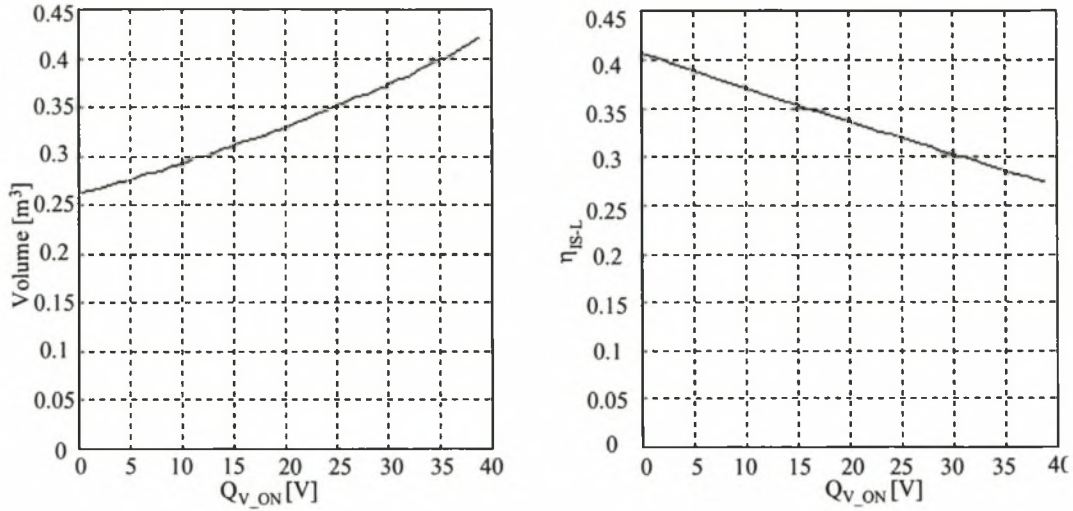


Fig. 5-1 Volume and η_{IS-L} vs Q_{V_ON}

It appears therefore that the dependence of the system volume on $Q_{V_ON}(n)$ is cancelled by its equal dependence on the series configuration of the IS.

Fig. 5-1 is calculated for a $k_{\Omega} = 1$; $t_{rat} = 1.5$; $s_{BP} = 80 \text{ kW/l}$, $t_d = 5 \text{ ms}$ and a copper inductor. Also, the ratio $\lambda_r = 1.5$ still holds. It is clear that the inclusion of Q_{V_ON} does affect the system volume appreciably, as indicated in Fig. 5-1; a realistic value of 20V will increase the volume by 27%.

The assumption made in the rest of this section, however, is that the continuous model should be used in order to gain an understanding as to the general dependence of the volume on the selected parameters. Thus for sections 5.5 to 5.8, it is assumed that Q_{V_ON} is zero unless otherwise stated; from this general results can be drawn. If it is required to include the dependence of specific parameters on Q_{V_ON} , then a rough estimate can be gained from a percentage multiplier derived from Fig. 5-1. Furthermore, if the exact technology is known – for the battery unit volume and switch on-state voltage – the discrete model can be used to obtain realistic system volumes.

5.5 Dependence of volume and η_{IS-L} on E_{STORED}

In order to observe the volume and η_{IS-L} dependence on E_{STORED} the assumptions made are $\lambda_r=1.5$; $k_\Omega = 1$; $s_{BP} = 80 \text{ kW/l}$ and the inductor is copper.

From Eq. 4-30 the system volume is dependent on the energy stored by the equation

$$VOL_{TOT} = E_{STORED}^{\frac{3}{5}} \cdot f(\rho_{metal}, s_{BP}, k_\Omega, t_{ra}, \lambda_r). \quad 5-14$$

Graphically this is represented by Fig. 5-2.

With the understanding that the switch volume increases with the current and thus with the square root of the energy, it is possible to calculate the switch volume dependence on stored energy separately (and independently) with the use of Eq. 4-30.

This is not considered further here.

The transfer efficiency is

$$\eta_{IS-L} = \frac{E_{STORED}}{E_{STORED} + E_{DISSIPATED}}, \quad 5-15$$

where the individual terms are discussed in section 4.5.8. The result is

$$\begin{aligned} \eta_{IS-L_no_switch} &= \frac{\frac{I_{REQ}^2 L_{ST}}{2}}{\frac{I_{REQ}^2 L_{ST}}{2} + \frac{I_{REQ}^2 L_{ST}}{(1 - e^{-t_{rat}})^2} \cdot (4e^{-t_{rat}} + 2t_{rat} - e^{-2t_{rat}} - 3)} \\ &= \frac{(1 - e^{-t_{rat}})^2}{2(e^{-t_{rat}} + t_{rat} - 1)} \end{aligned} \quad 5-16$$

which shows that if the switch energy dissipation is ignored, the front-end transfer efficiency remains independent of the amount of energy stored (it is set at 0.42 for all the energies). According to Fig. 5-1, the dependence of this efficiency on Q_{V_ON} is evident. At 500 kJ and $Q_{V_ON} = 20$ (chosen arbitrarily) the efficiency is brought down to 0.34; the efficiency improves towards 0.42 as the energy increases.

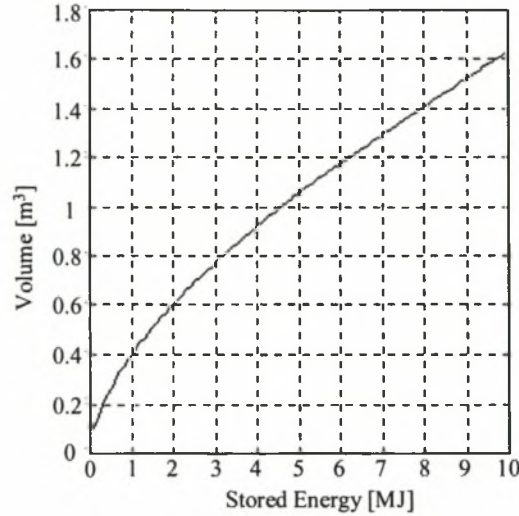


Fig. 5-2 Volume vs. E_{STORED}

5.6 Dependence of volume and $\eta_{\text{IS-L}}$ on s_{BP}

In order to observe the volume and $\eta_{\text{IS-L}}$ dependence on s_{BP} the assumptions made are $\lambda_r = 1.5$; $k_{\Omega} = 1$; $t_{\text{rat}} = 1.5$; $E_{\text{STORED}} = 500 \text{ kJ}$ and the inductor is copper.

From Eq. 4-30 it is shown that the volume is dependent on the battery specific power density by the equation

$$VOL_{\text{TOT}} = s_{\text{BP}}^{-\frac{3}{5}} \cdot f(\rho_{\text{metal}}, E_{\text{STORED}}, k_{\Omega}, t_{\text{RAT}}, \lambda_r). \quad 5-17$$

This is demonstrated graphically in Fig. 5-3.

Eq. 5-17 shows that the system efficiency is independent of the battery power density (assuming all the other factors are held constant) if the switch dissipation is ignored. The efficiency is just below 0.42. Inclusion of the switch energy dissipation results in a decrease in system efficiency (as expected). At 80 kW/l and $Q_{V_ON} = 20$ (chosen arbitrarily) the efficiency is brought down to 0.34; the efficiency improves towards 0.42 as battery power density increases. Thus the higher the power density, the less is the effect of the switch loss on system efficiency.

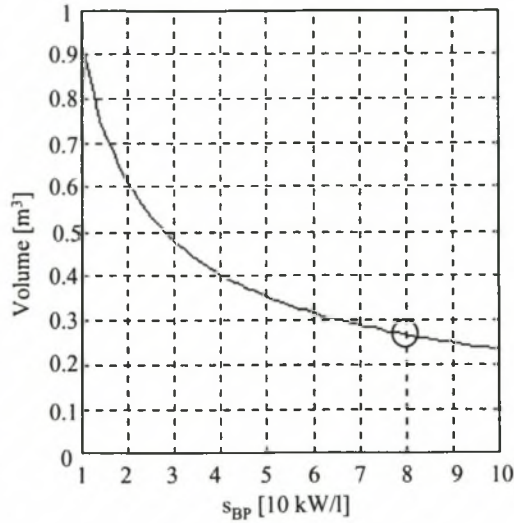


Fig. 5-3 Volume and η_{IS-L} vs. s_{BP}

5.7 Dependence of volume and η_{IS-L} on t_{rat}

In order to observe the volume and η_{IS-L} dependence on t_{rat} the assumptions made are $\lambda_r=1.5$; $k_{\Omega}=1$; $s_{BP}=80 \text{ kW/l}$; $E_{STORED}=500 \text{ kJ}$ and the inductor is copper.

The significance of this variable is not initially clear; it is included in this discussion to allow for correlation of these results to those documented in [10]. The charge time ratio is the ratio of the charge time t_{CH} to the front-end time constant t_{Const} ; thus a charge time ratio of x means that the system is charged for x front-end time constants.

Eq. 4-30 gives the relation.

$$VOL_{TOT} = \left(1 - e^{-t_{rat}}\right)^{\frac{6}{5}} \cdot f(\rho_{metal}, E_{STORED}, s_{BP}, k_{\Omega}, \lambda_r). \quad 5-18$$

This is demonstrated graphically in Fig. 5-4.

In order to better appreciate the relation of the charge time ratio to the system, the system efficiency is considered. Eq. 5-16 gives a clear indication of the dependence of η_{IS-L} on t_{rat} . Comparison of Fig. 5-4 shows that while there is little gain in the decrease of the system volume as t_{rat} passes 2, there is a definite decrease in system efficiency.

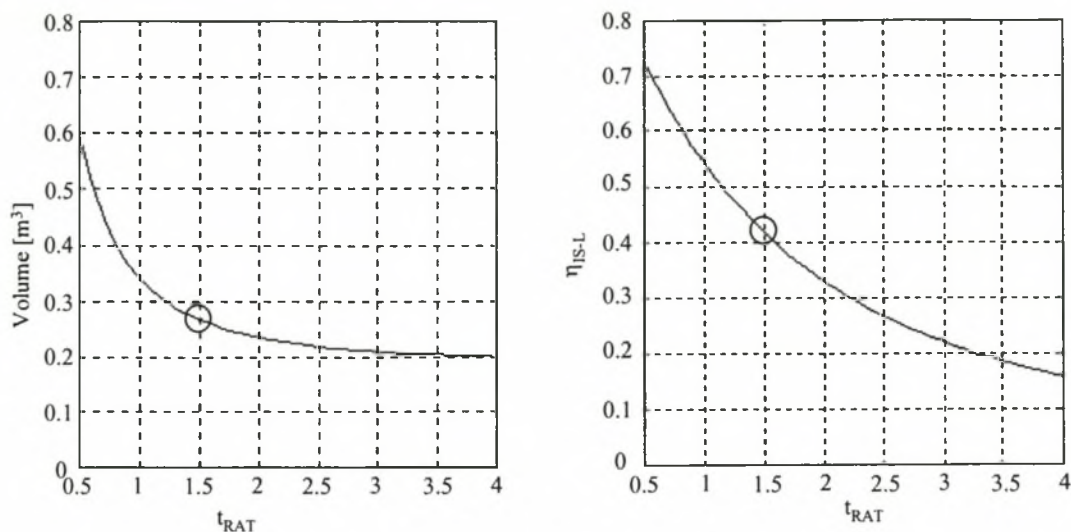


Fig. 5-4 Volume and η_{IS-L} vs t_{rat}

5.8 Dependence of volume and η_{IS-L} on t_{CH}

In order to observe the volume and η_{IS-L} dependence on t_{CH} , the assumptions made are $\lambda_r=1.5$; $k_{\Omega} = 1$; $s_{BP} = 80 \text{ kW/l}$; $E_{STORED} = 500 \text{ kJ}$ and the inductor is copper.

The continuous model and Eq. 4-30 are not suited to this calculation (as there is a coupled dependence on t_{Const} that can not be incorporated). Alternatively, the discrete model is used in this section. Effectively, the inductor value is held constant as the

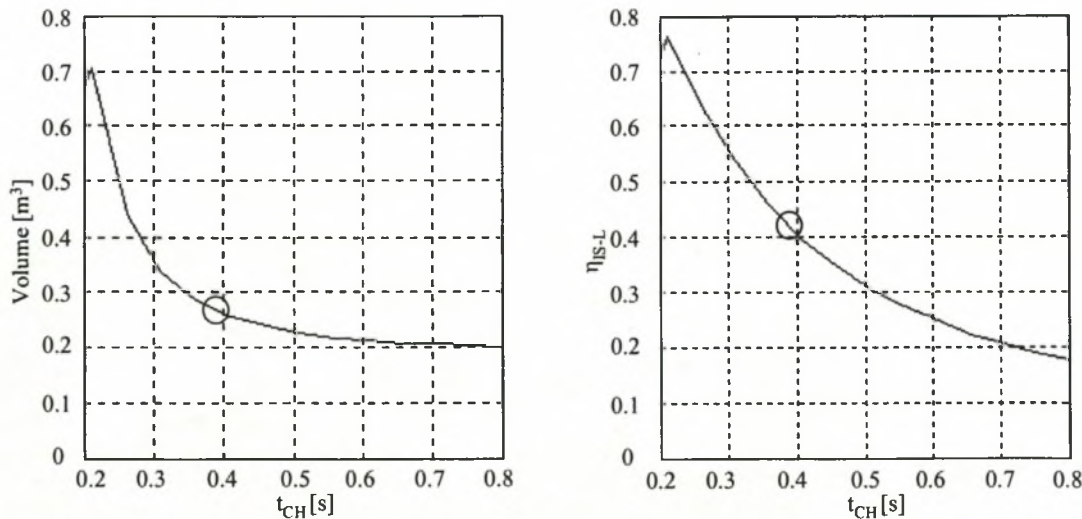


Fig. 5-5 Volume and η_{IS-L} vs. t_{CH}

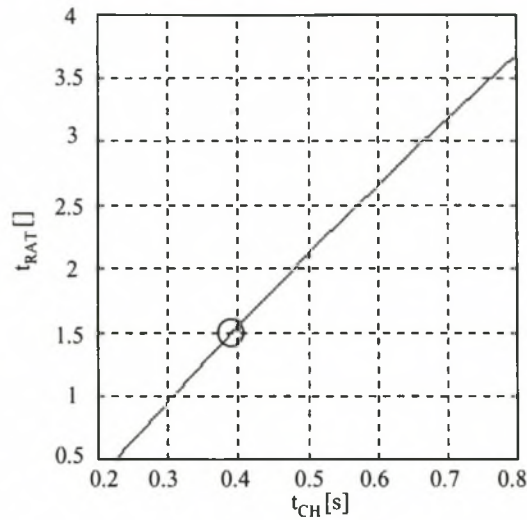


Fig. 5-6 t_{RAT} vs t_{CH}

calculations sweep through the desired charge times; the charge time ratios t_{rat} will also vary. Fig. 5-5 shows the dependence of the system volume and front-end efficiency on the charge time. Fig. 5-6 shows the relation between t_{CH} and t_{rat} .

5.9 500 kJ system suggestion

A system suggestion is made in this section. Most of the figures in this chapter have a marker placed on a point in the graph. This relates to the system suggestion used in this section.

5.9.1 Battery technology

The battery technology chosen is that documented in Ref. [10]. It is a Bolder thin-metal foil (TMF) battery with a power density of 80 kW/l or a delivered power density to a matched load of 20 kW/l.

5.9.2 Inductor technology

1. The Brooks coil allows for optimum energy density and is adopted throughout.
2. Ref. [9] and section 4.5.5 discuss various back-end transfer efficiency considerations. These are ignored here and $\eta_{L-load}=1$.
3. Ref. [10] considers inductor strength requirements; it is shown that if used in a volume-optimised procedure as discussed here, the inductor requires no extra strengthening; the material's own tensile strength is sufficient to support the inductor.

4. Temperature considerations may be an issue. Using the volume model proposed and calculating the energy dissipated in the inductor per shot, it is shown in section 4.5.8 that the temperature rise is never more than 6°C per firing cycle. Assuming sufficient heat-exchange is implemented, no extra hardware requirements need to be implemented.
5. For an aluminium inductor system, the IS-L volume minimum occurs at 0.36 m³. For copper-based systems, the minimum occurs at 0.26 m³. The copper-based system is chosen.

5.9.3 Switch technology

A major focus of this research is on the application of solid-state switch technology.

An inductive storage supply requires an opening switch capable of conducting the full load current during the charge cycle and holding the load voltage during the discharge cycle. Table 5-2 and Table 5-3 describe the relevant aspects of the available high-power turn-off solid-state switches applicable to millisecond inductive storage PFNs. Due to the very limited data available on the pulse characteristics of these devices, some assumptions have to be made. These are described in section 4.2.2. Of most importance is the maximum allowable current per device. This is given [74] as

$$I_{COND} = \frac{\Delta T_{jc}}{V_{ON} R_{\theta}}, \quad 5-19$$

with ΔT_{jc} the junction-case temperature difference, V_{ON} the device on-state voltage, R_{θ} the device junction-case thermal resistance and I_{COND} the maximum allowable device current. ΔT_{jc} is set at 100°C.

Table 5-2 Switch technology suggestions and device volume

<i>Device</i>	<i>HVIGBT</i>	<i>HVIGBT</i>	<i>GCT</i>	<i>GTO</i>
Ratings / unit	3.3kV 1.2kA	6.5kV 600A	4.5kV 4kA	6kV 6kA
Part number	CM1200HB-66H	FZ600R65KF1 (Eupec device)	FGC4000BX-90DS	FG6000AU-120D
Package	Top-mounted	Top-mounted	Hockey puck	Hockey Puck
T _{OFF}	1μs	4μs(waveform)	Not given	30μs
RMS on-state rated current	Not given	Not given	1880 A	3100 A
R _{Thermal j-c} °C/W	0.008	0.0105	Not given	Not given
R _{Thermal c-f} °C/W	0.006 (with grease)	0.006 (with grease)	Not given	Not given
R _{Thermal j-f} °C/W	0.014	0.0165	0.011	0.0044
With driver	<i>an</i>	<i>an</i>	0.012 (GU-C40)	Not Given
V _{ON} (typ./max.)	3.8 / 4.94	5	Not given / 4 V	Not given / 6 V
Max. current (calculated)	1880 A	1212 A ^s	2272 A	3780 A
Unit Volume	1.1 litre	1.3 litre	0.45 litre	1.3 litre
Unit Volume with driver	+ 2 litre	+ 2 litre	3 litre *	6 litre **
80 kA / 20 kV switch?	80 kA / 1880 × 20 kV / 3.3 kV	80 kA / 1212 × 20 kV / 6.5 kV	80 kA / 2272 × 20 kV / 4.5 kV	80 kA / 3780 × 20 kV / 6 kV
	43×6 (19.8kV)	66×4 (26 kV)	36×5 (22.5kV)	21 × 4 (24kV)
Device ***	516 litre	528 litre	540 litre	504 litre
Snubber ****	130 litre	130 litre	270 litre	250 litre

Refer to Table 5-3 for the superscript discussions

This is only a first-order approximation; more detailed study into the thermal considerations of the silicon device and possible device over-rating is required (not considered further in this research). The device volumes shown in Table 5-2 are an approximation based on contemporary devices in their standard packaging. The

tabulated values are meant only as a guideline. Only basic sharing hardware volume considerations have been implemented. If capacitive sharing is to be implemented (as performed with the scale model), the device volume could easily double. However, a number of active-sharing schemes (Appendix E) exist (particularly for IGBTs) that could be implemented as part of the driver with little or no extra volume cost.

Table 5-3 Device heatsink requirements

<i>Device</i>	<i>HVIGBT</i>	<i>HVIGBT</i>	<i>GCT</i>	<i>GTO</i>
V_{ON}	$6\mu \times 5 = 30 \text{ V}$	$4 \times 5 = 20 \text{ V}$	$5 \times 4 = 20 \text{ V}$	$4 \times 6 = 24 \text{ V}$
Energy/ ^{ss} 400ms, $t_{RAT} = 1.5$	600 kJ	400 kJ	300 kJ	480 kJ
P_{AVE} (0.1 Hz)	60 kW	40 kW	30 kW	48 kW
Heatsink tech. $T_{s-a} = 30^\circ\text{C}$	Semikron P16/300 $R_\theta = 0.031$ 1kW / 5l	Semikron P16/300 $R_\theta = 0.031$ 1kW / 5l	Semikron U3/300 $R_\theta = 0.04$ 1kW / 15l	Semikron U3/300 $R_\theta = 0.04$ 1kW / 15l
Heatsink volume *****	300 l	200 l	450 l	720 l

^s Value calculated like normal; it appears that the device is necessarily underrated.

^{ss} Using Eq. 4-62 and excluding switching losses

* GU-C40. specified. Excluding isolated dual 15V 10A supply required

** Assuming GU-C40 dimensions $\times 2$

*** Assuming no capacitive snubbing; specs are silicon and driver only

**** Capacitive snubbing. For IGBT = 0.25 device volume. For GTO-based, = half device volume

***** Assuming that the heatsink is force air-cooled and equally distributed amongst the switches

Of importance is the total current chosen. This value is assumed from correspondence with the contractor from January 2000. As is observed later, the actual required current level for the suggested system is about half of this. Thus the values tabulated in the above and the following table are for an 80 kA system. Those calculated for the suggested system are for a 40 kA system. Thus it is a very sensitive function of the required discharge time t_d and load approximation R_L according to Eq. 4-54 that determines I_{req} and as a result the required switch volume.

It is observed that (excluding heat sink volume requirements), the four technologies considered all allow for similar switch volume requirements. However, taking heatsink volumes into consideration (using industry standard heat-sinking) it is observed that the HVIGBT technology is superior; however, this is very rough estimate. Not taken into account are other considerations that are particularly device specific; factors such as switching speed, switching method and ease, switching losses and potential EMI considerations are the major ones. IGBTs, however, are well recognised to be the device of choice in applications where they are applicable as they are superior to the GTO family in most aspects.

Also, series sharing of devices is a definite issue. The statistics tabulated here do not take any sharing into account for the device volume considerations. Although capacitive-only sharing is potentially the most robust form of voltage sharing (as implemented in the prototype), the added volume requirements force the designer to consider alternatives. Appendix E presents some active and alternative passive methods to implement voltage sharing that result in little or no increase in device volume. It is assumed that these methods are implemented and no extra device volume is required.

5.9.4 System and subsystem specifics and results

Correlation of the data from section 5.7 shows that while a slight decrease in system volume is achieved as the t_{RAT} value exceeds 1.5, the system efficiency drops appreciably. It is possible to determine some sort of cost function relationship to determine the desirable t_{RAT} , dependent possibly on the energy storage capacity of the IS, heat exchange within the inductor, or the desirable charge time, dependent on system specifications. The following system is a potential option. Table 5-4 tabulates the system specifics for a 4-module 500 kJ system. $Q_{V_ON} = 20\text{V}$ has been brought into the calculation. Table 5-5 shows the important system considerations with focus on the ideal (excluding switch) and real (including switch) values.

Table 5-4 500 kJ system suggestion specifics

Module count N	4
Discharge time t_d	5 ms
Inductor value L_{TOT}	8 mH
Required charge current I_{REQ}	11 800 A
IS voltage and current	460 V short circuit current of 35 kA
Effective charge time t_{CH}	455 ms
Total current (used for switch volume)	45 000A
Inductor ESR L_{ESR}	13.2 mΩ
Inductor winding number	120
Conductor diameter	2 cm

Table 5-5 500 kJ system volume and efficiency

	$IS_{VOL}+L_{VOL}$	t_{CH}	t_{rat}	η_{IS-L}
Without switch	0.26 m ³	400 ms	1.5	0.42 (exc. switch)
With switch*	0.333 m ³	450 ms	1.5	0.34
Q_{VOL} *	$(0.528+0.13+0.20) \times 45 / 80 = 0.480 \text{ m}^3$			
TOTAL	$0.333 + 0.480 = 0.813 \text{ m}^3$			

* Using FZ600R65KF1 and $Q_{V_ON} = 20 \text{ V}$ and adjusting for reduced current requirement

The inductor specifics listed in Table 5-4 need to be incorporated into a usable device. Using the method of inductor modelling described in section 4.2.5 and the assumption of balanced modules as outlined in section 4.2.4, it is possible to define the inductor dimensions and coupling specifically. No isolation considerations are made.

The inductor has a winding count of 120. Allowing for some deviation from the exact Brooks configuration, the inductor is wound as 12 Pancake Coils (PCC) of 10 windings each that are mounted directly upon one another. A pancake coil is one that is wound in a horizontal plane and appears flat. This method is assumed as it allows for comparatively simple processing of \mathbf{M}_N (which for this system is a 120×120 matrix) to represent a balanced four-module (4×4) system.

The final inductor volume is 0.15 m^3 , which is just above that required by the optimisation procedure (a slight volume increase is required to compensate for the non-Brooks dimensions).

Table 5-6 500 kJ inductor normalised inductance values

Module #	1	2	3	4
1	1	0.9	0.86	0.84
2	0.90	1	0.9	0.86
3	0.86	0.90	1	0.9
4	0.84	0.86	0.90	1

All values are normalised to 550 μH . Total inductance = 7.95 mH

5.10 Summary

This chapter analyses the volume models proposed in Chapter 4 and clarifies the dependence of the system volume and efficiency on E_{STORED} , S_{BP} , t_{rat} , t_{CH} , t_d , system modularity, switch volume and Q_{V_ON} .

Due to the as yet unclear specifications of a final system and its requirements, this generalised approach – of simply recognising and defining the volume dependence on some designer-controlled factors – is considered best.

The inclusion of Q_{V_ON} into the design procedure indicates that its effect is not negligible. Also, it is not possible to include Q_{V_ON} into the continuous model and the alternative – the discrete model discussed in this and the previous chapter – is required to obtain results.

The approach assumed here is that generalised results and dependencies discussed in sections 4.3.4, 5.2, 5.3 and 5.5 to 5.8 that are mostly deduced from the continuous model are used for initial system considerations (all excluding the effects of Q_{V_ON}).

For quantified system values – when specific technologies are recognised and implemented –the discrete model incorporating the effect of Q_{V_ON} can be used.

A system example is given using technologies specified in the relevant sections. It is clear that a system of volume under 1 m^3 is possible. This discussion is re-approached in the closing chapter of this report, however.

An important point is the high dependence of the switch volume on the required discharge time t_d as demonstrated in Eq. 4-55; the inductor and IS volume are independent of this value (as discussed in section 4.5.5). Definition of this time is subject to the designer. It is proven in section 3.3 that balanced inductors are required. The choice of required discharge time is a criterion assumed in this project.

CHAPTER 6

PROTOTYPE RESULTS

6.1 Introduction

Design, construction and testing of a prototype are presented in this chapter. The original contract specifies a 2.5 kV, 1.2 kA system. No specific pulse shaping or energy requirements are specified. The prototype design decisions follow the following route:

1. A minimum t_d of 1.3 ms is assumed.
2. Section 3.3 considers a module count of 4 as optimum.
3. For a load current of 1.2 kA, the four modules require a charging current of 300A.
4. For a load voltage of 2.4 kV, a 2Ω load is required.
5. The required inductor value (Eq. 4-53) is 42 mH.
6. It is observed from section 3.3 that a balanced inductor system is required for a volume optimum.
7. The IS is composed of readily available batteries.
8. The switches are required to conduct 300 A ($1200 \text{ A} / 4$) for the required charge time and hold the full load voltage when off.
9. Charge time specifications would typically require some type of efficiency optimisation, as demonstrated in section 5.8. As efficiency is not directly an issue in the prototype, a typical charge time of 300 ms is arbitrarily chosen.

The focus of the prototype construction is to research the applicability of IGBTs to the topology, validate the topology itself and to demonstrate the volume optimisation algorithm. However, use of the design algorithms proposed in section 4.3 results in a number of practical difficulties. These are presented and model modifications (and the resultant ramifications) are discussed. A final system meeting the design requirements is proposed, constructed and tested.

The more relevant construction specifics – particularly involving the inductor design and switch bank design – are also presented.

Lastly, some results are documented and discussed.

6.2 Volume model modifications

The *continuous* model of section 4.3 gives general results (such as front-end matching, $\lambda_r = 1.5$) and gives volume optimums for continuous values of s_{BP} . However, the continuous model is not suited to the inclusion of Q_{V_ON} into the optimisation procedure. Furthermore, *IS* dimension relations are not defined. That is, the *IS* is actually composed of a bus of N_p parallel units and N_s series units, each a dimensionless number.

Table 6-1 Volume protocol results

	<i>Matched</i> ^{**}	<i>Matched</i> ^{***} <i>with Q_{V_ON}</i>	<i>With</i> ^{***} $k_\Omega \neq 1$	<i>With</i> ^{***} $k_\Omega \neq 1$ <i>and Q_{V_ON}</i>
System	1	2	3	4
VOL_{TOT}^{\S}	36 l	43 l	86 l	109 l
L_{VOL}	15 l	17 l	38 l	45 l
IS_{VOL}	21 l	26 l	48 l	64 l
Q_{VOL}	32 l	32 l	32 l	32 l
k_Ω	1	1	7.5	5
t_{CH}	0.3 s	0.32 s	0.31 s	0.3 s
t_{rat}	4.2	4.4	1.36	1.22
N	390	386	335	325
N_s	15	16	6	8
N_p	0.1775	0.2205	1	1
L_{ESR_TOT}	0.3 Ω	0.275 Ω	0.158 Ω	0.141 Ω
IS_{ESR}	0.3 Ω	0.275 Ω	0.021 Ω	0.028 Ω
L_{rad}	0.22 m	0.22 m	0.29 m	0.31 m
δ	0.535 cm	0.557 cm	0.79 cm	0.85 cm
L_{COND_AREA}	22.5 mm ²	24 mm ²	49 mm ²	57 mm ²
ΔT_L	0.26 K	0.25 K	0.06 K	0.04 K

^{*} Using Espace 45G model with $Batt_{VOL} = 8/$ and $Batt_{ESR} = 3.5 \text{ m}\Omega$

^{**} Continuous or discrete model

^{***} Discrete model

^{\S} Excluding switch volume

It is shown in Chapter 4 that the module number does not effect overall system volumes, but it does effect the parallel and series makeup of the *IS*. As a result of this, the assumption of a continuous s_{BP} , although useful for overall volume calculations, exercises limited control over the actual series or parallel *IS* makeup.

Low-energy systems or the utilisation of high energy density batteries could result in the requirement of non-integer battery number requirements; this is a potential problem for practical systems. The *discrete* model addresses these shortcomings.

For a matched load and continuous s_{BP} , the results of the discrete model exactly match those of the continuous model (using the correct constant of section 5.1) with $Q_{V_ON} = 0$. However, use of the discrete model with front-end matching could still produce impractical results (such as a partial battery volume requirements).

If this proves to be a problem, the discrete model can be used to force the *IS* to be composed of only discrete unit values. However, examination of Eq. 4-28 shows that this forces a non-continuous value of s_{BP} , and effectively limits the possible IS_{ESR} values to a few discrete values (while the inductor is still capable of any L_{ESR_TOT}).

It is understandable therefore that the volume minimum can occur at some resistance relation $k_{\Omega} \neq 1$. This has the implication that the continuous model is no longer valid under these conditions. Although not proven formally, it is assumed that use of k_{Ω} as the iteration parameter (running through a series of k_{Ω} for each possible combination of discrete N_P and N_S) will still result in a practical system minimum, although this minimum will necessarily be higher than that assuming a continuous s_{BP} and a matched front-end.

The discrete model is thus further divided into the *matched* and the *unmatched* cases.

It is observed in systems 1 and 2 of Table 6-1 that the required battery combination is impractical and requires partial battery volumes. This is because the required current is far below the rated short circuit current of the device; as discussed, this is peculiar to low-energy systems or systems incorporating specific power batteries. Systems 3 and 4 show results using the *unmatched* discrete model that uses the resistance relation modifier, k_{Ω} , as a design iteration tool and the required charge time t_{CH} as the iteration objective. This will provide a less than optimum volume assuming a continuous s_{BP} , but will provide for a minimum practical system volume.

Inclusion of the switch on-state voltage (where $Q_{V_ON} = 6V$ for each module switch in the simulation) also results in appreciable system volume differences.

6.3 Finalised results from volume model

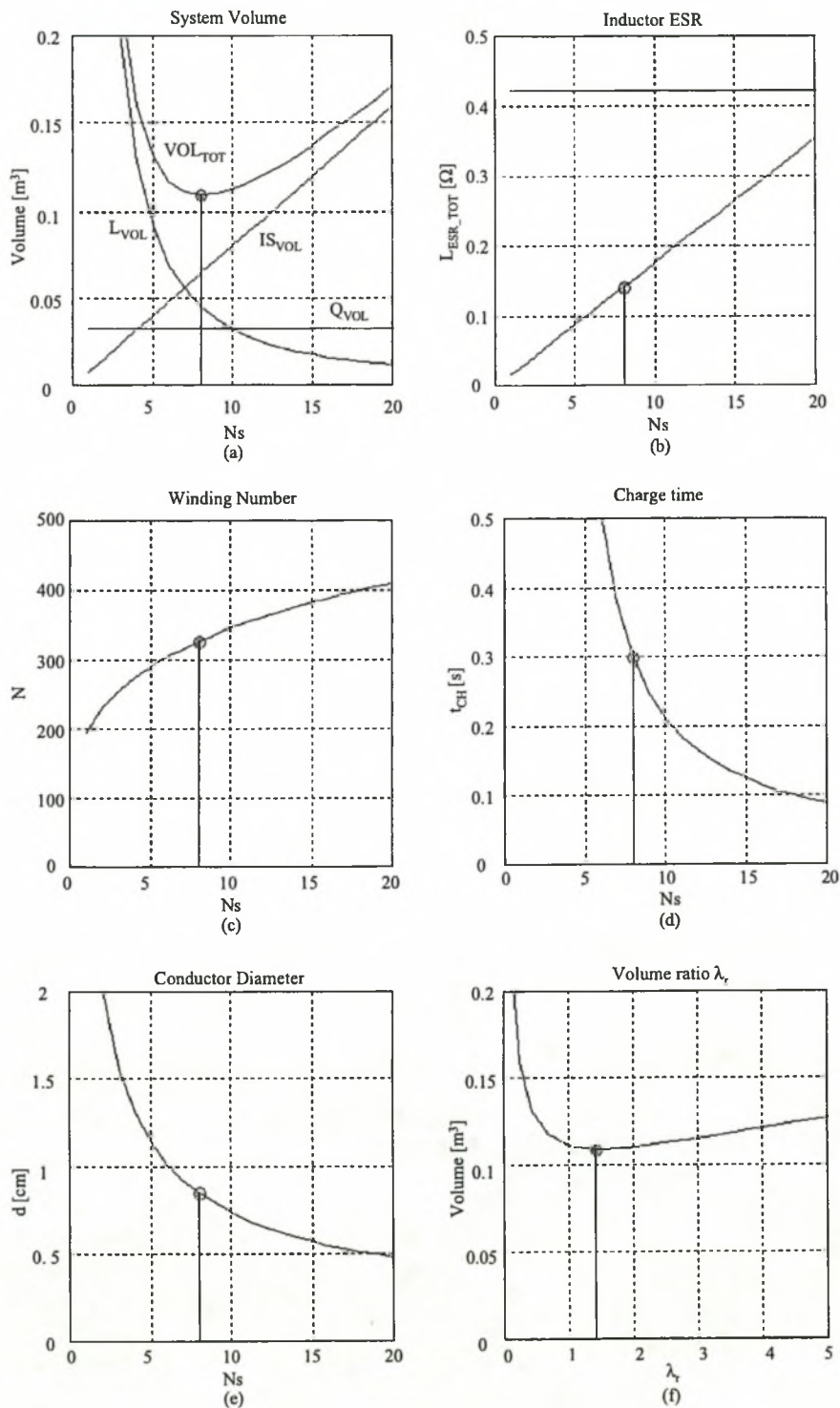


Fig. 6-1 Discrete model with $k_\Omega \neq 1$, $N_P = 1$ and Q_{V_ON} compensation

Fig. 6-1 shows the typical outputs of the discrete model tabulated in Table 6-1; the actual represented system is that of system 4. Not included in Fig. 6-1 are the inductor temperature, charge ratio t_{rat} and inductor diameter graphs that are also generated by the Matlab simulation but are omitted here. All the information tabulated in Table 6-1 is read directly from such graphs for the relevant simulations with the relevant models. The resultant volume tabulated in Table 6-1 column 4 will not be the volume minimum (that is possible with a continuous IS), but will result in the minimum volume of a practical system; λ_r still retains a value close to 1.5.

Fig. 6-1(a)

This is the volume result. Shown in this result is the IS volume (as it linearly grows with a constant N_p and linearly changing N_s) and the inductor volume, calculated from some power matching relation of the front-end. For the matched system solution, N_p is also changed during the simulation, but only the last – and optimum – N_p is used to generate results that are displayed. It is also clear that the switch volume remains constant. A volume minimum clearly results.

Fig. 6-1(b)

L_{ESR_TOT} is displayed here. The solid transverse line indicates the maximum allowable ESR to result in minimum allowed back-end efficiency for a series discharge. It is used as a check; the transfer efficiency limit is set at 0.95.

Fig. 6-1(c)

Winding number of the required inductor.

Fig. 6-1(d)

Resultant front-end charge time t_{CH} of the system; it is used in this system as the iteration goal and set at 300 ms.

Fig. 6-1(e)

This is the required conductor diameter. It is used for inductor construction information. Inductor dimensions such as the inner radius are also generated in a similar graph (not shown here).

Fig. 6-1(f)

The volume ratio λ_r , faithfully remaining at 1.5 despite the fact that the mathematics appears to render the continuous model inapplicable. Throughout Fig. 6-1 a stem plot shows the minimum volume and resultant system parameters that are required for this minimum.

6.4 Constructed system parameters

Construction of the system as tabulated in Table 6-2 differs from the theoretical predictions of Table 6-1.

Table 6-2 Constructed system volume

<i>System volume</i>	<i>204 l</i>
Inductor volume	100 l
Battery volume	72 l
Switch volume	32 l
Number of batteries	9 = 108 V
Winding number of Brooks coil	256
Inductor dimensions	Brooks Dimension c = 20 cm
Inductor conductor dimensions	area = 0.5cm ²
Inductor conductor length	520 m
Inductor ESR	187 mΩ

The main difference is in the inductor characteristics. Practical issues resulted in the construction of the inductor using Permoweld with 0.5 cm² conduction area and bulky 1 kV isolation. Due to the modular nature of the inductor, inter-conductor isolation should match the load. Thus two adjacent cables will be specified at 2 kV. It is understood that this value is under-rated and that higher voltage isolation – especially at pulse time-scales – is viable.

The resultant L_{ESR_TOT} is higher than that required and the constructed inductor value is also lower than expected.

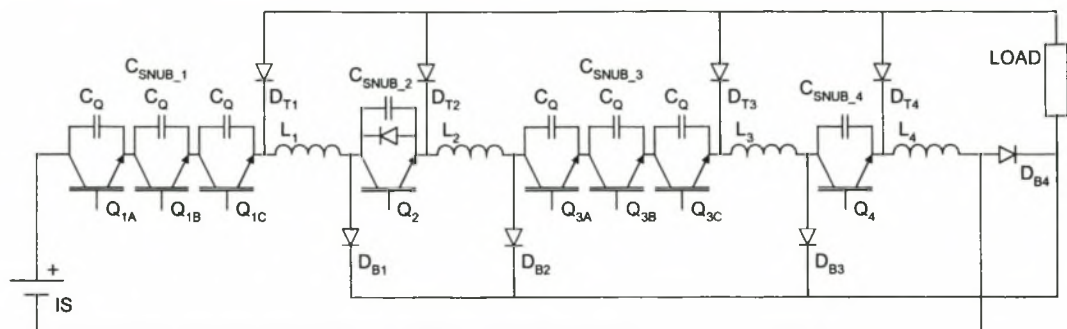


Fig. 6-2 Full XRAM topology showing active components

Table 6-3 XRAM topology breakdown

Device	Description
Q ₁ , Q ₃	Powerex (Mitsubishi) CM400HU-24F. Module is a discrete IGBT with anti-parallel diode. Technology is trench-gate which allows low on state voltage (1.7 V at 300 A). Three are used in series to build up the required 2.5 kV. Device × 6, each rated at 1.2 kV and 400 A.
Q ₂ , Q ₄	Powerex (Mitsubishi) CM400DY-66H. Module is a dual pack (isolated) with anti-parallel diode per device. Device × 1, each rated at 3.3 kV and 400 A. Anti-parallel diode of Q ₂ conducts for a short while during the charge cycle; the others do not play a role.
Drivers	The standard Mitsubishi M57962L driver is used.
D _{TX}	Semikron SKND150F12. Dual anode to anode diode module. Device ×2.
D _{BX}	Semikron SKMD 150F12. Dual cathode to cathode diode module. Device ×2.
L _{1..4}	Single brooks coil. 256 windings with four isolated and balanced modules. 0.5cm ² Permoweld cable and air-core. Module self inductance = 2.1 mH.
IS	Espace 45 G with 12V, 8 l and 3.5 mΩ per unit. 9 units used.
Load	Salt water load. CuSO ₄ solution.
C _{SNUB_1,3}	Each full sharing snubber set composed of three C _Q . Each C _Q composed of two parallel IECL 2μF 1000V box caps. No sharing resistors required.
C _{SNUB_2,4}	Single Siemens MKV 0.22 μF, 3.4 kV GTO snubber cap.

Fig. 6-2 shows the full XRAM topology of the prototype. Further component descriptions are given in Table 6-3.

6.5 Inductor construction

Practically, the inductor posed a challenge. It is large and correspondingly heavy, has an air-core and must be electrically modular. The Permoweld was chosen due to the ease of construction it would allow. The winding method chosen was to allow for a great deal of flexibility; 16 PCC layers were considered the best suited to all of these requirements. The winding number of each layer was reduced from 17 to 16 during construction. Final inductor dimensions fit those shown in Fig. 6-3.

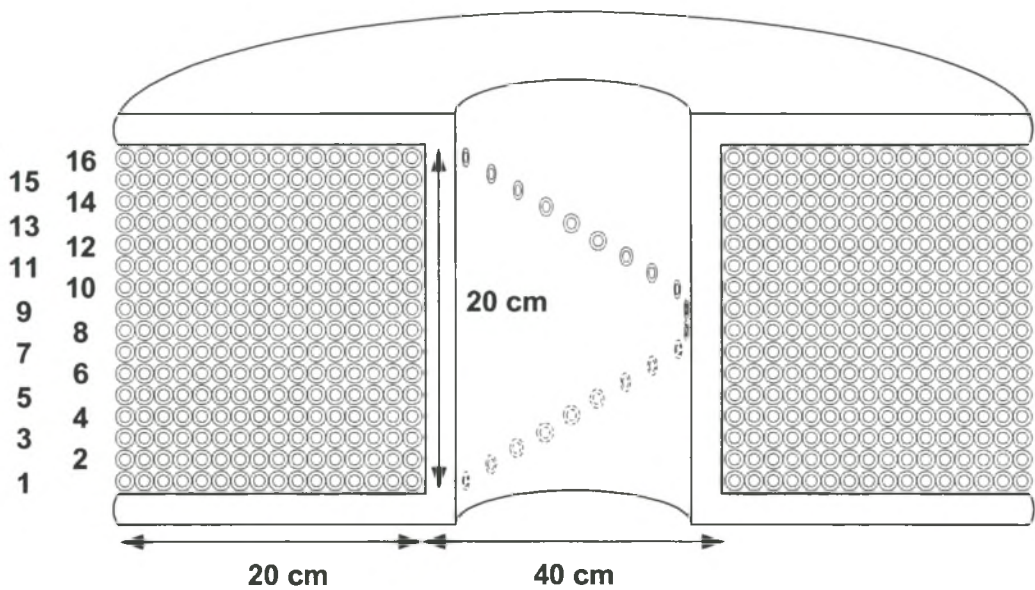


Fig. 6-3 Inductor dimensions with PCC numbering

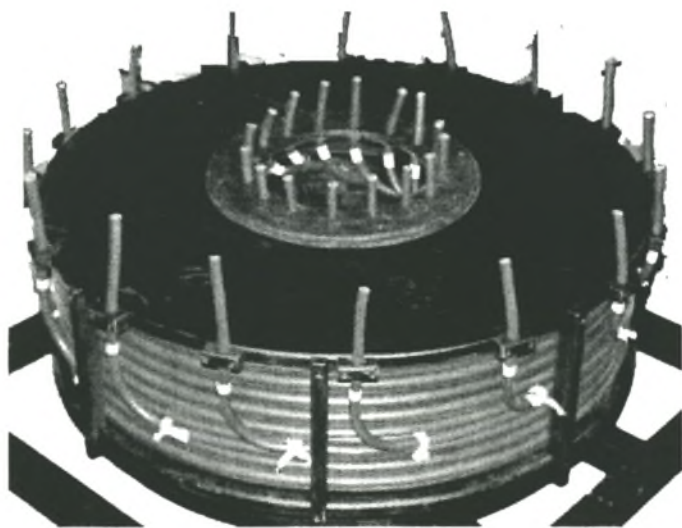


Fig. 6-4 Actual constructed inductor

Inductor construction up to the stage depicted in Fig. 6-4 was performed through a private contractor. At this stage it is possible to determine the desirable PCC connections. In order to do so, the full inductor with its 256 coils can be modelled as an inductance matrix of $\mathbf{M}_{256 \times 256}$ (section 4.2.5). Next, the 16 PCC coils were formed, which resulted in the PCC matrix of form $\mathbf{M}_{16 \times 16}$, with the diagonal representing each PCC self inductance and being equal, through symmetry. It is clear from simple symmetry arguments that to generate the required balanced \mathbf{M}_n (section 4.2.5) where $n = 4$, a simple series connection of the form tabulated in Table 6-4 is sufficient.

Table 6-4 Inductor module connections

Module 1	1	5	9	13
Module 2	2	6	10	14
Module 3	3	7	11	15
Module 4	4	8	12	16

Table 6-5 Inductance values (calculated / measured) [mH]

Module	1	2	3	4
1	2.11 / 1.96	1.98 / 1.94	1.93 / 1.88	1.91 / 1.86
2	1.98 / 1.94	2.11 / 2.00	1.98 / 1.95	1.93 / 1.91
3	1.93 / 1.88	1.98 / 1.95	2.11 / 1.96	1.98 / 1.94
4	1.91 / 1.86	1.93 / 1.91	1.98 / 1.94	2.11 / 2.00
total	32 mH			

Table 6-6 Coupling factors (calculated / measured)

Module	1	2	3	4
1				
2	0.94 / 0.98			
3	0.91 / 0.96	0.94 / 0.98		
4	0.91 / 0.94	0.91 / 0.95	0.94 / 0.95	

The resultant measured and calculated inductance values of Table 6-5 are in reasonable agreement, with a 90% accuracy worst case. The reduction of the total

inductance value – from 42 mH to 32 mH – is as a result of the structural changes (the calculated values simulate the constructed inductor).

6.6 Switch bank construction

6.6.1 Device details and heatsink design

Heat sinking of the full commissioned system is worst case. Thermal steady-state considerations have little meaning, as the fire-repetition rate is around 8 shots per min; substantial heat-cycling will occur in this time frame.

Furthermore, exact thermal steady-state measurements of the prototype are not considered a prime criterion. However, the heatsink is required for simply mounting of the devices and a heatsink design is performed. Assuming that the heatsink is at a temperature with temperature difference of ΔT_{sa} sink to ambient, an average power output can be calculated.

Table 6-7 Device specifications

<i>Parameter</i>	<i>CM400HU 24F</i> <i>discrete</i>	<i>CM400DY 66H</i> <i>Discrete</i>	<i>SKMD 150 F12</i> <i>SKND 150 F12</i>
Device type	Single	Isolated dual	dual
Rated V_{CE}	1200 V	3300 V	1200 V
Rated I_C	400 A	400 A	140 A
Peak I_C	800 A	800 A	2000 A in 10 ms
Q_{V_ON} at rated I_C	1.8 / 2.4 V	4.4 / 5.72 V	2.2 V
t_d (off) ; t_f ; t_{off}	0.6 / 0.3 / 0.9 μ s	2 / 1 / 3 μ s	na
R_θ	0.078 $^{\circ}\text{C}/\text{W}$	0.036 $^{\circ}\text{C}/\text{W}$	0.2 $^{\circ}\text{C}/\text{W}$
$R_\theta + R_{grease}$	0.098 $^{\circ}\text{C}/\text{W}$	0.052 $^{\circ}\text{C}/\text{W}$	0.25 $^{\circ}\text{C}/\text{W}$
V_{ISOL}	2500 V	5000 V	4000 V
ΔT_{js} for DC 300A	53 / 70 $^{\circ}\text{C}$	68 / 89 $^{\circ}\text{C}$	na
E_{OFF}	40 mJ	400 mJ	na

The energy transferred to a device during the conduction stage is

$$Q_{E_ON} = V_{CE} \cdot I_{final} \cdot \int_0^{t_{CH}} (1 - e^{-t/t_{const}}) \cdot dt$$

$$\Rightarrow Q_{E_ON} = V_{CE} \cdot I_{final} \left(t_{CH} - t_{const} + e^{-t_{CH}/t_{const}} t_{const} \right)$$
6-1

Assuming a worst-case charge cycle using three time constants, or a charge cycle with $t_{rat} = 3$, the energy transferred to the switch each cycle is

$$Q_{E_ON} = V_{CE} I_{final} t_{Const} (2 + e^{-3})$$

$$Q_{E_ON} = V_{CE} I_{req} t_{Const} \frac{(2 + e^{-3})}{(1 - e^{-3})},$$
6-2

where

$$I_{req} = I_{final} (1 - e^{-3}).$$
6-3

For a charge time of 300 ms and $t_{rat} = 3$, $t_{Const} = 100$ ms. The dissipated energy now equals

$$Q_{E_ON} = V_{CE} I_{req} t_{eff},$$
6-4

where $t_{eff} = 215$ ms.

Table 6-8 Switch conduction losses

Device	Losses
CM400HU-24F	$300 \text{ A} \times 2.4 \text{ V} \times 0.215 \text{ s} = 154.8 \text{ J}$
CM400DY-66H	$300 \text{ A} \times 4.29 \text{ V} \times 0.215 \text{ s} = 276 \text{ J}$

Comparison of the switching losses of Table 6-7 and the conduction losses of Table 6-8 indicate that the turn-off losses are effectively negligible. This is expected. The average power dissipation requirements per device is given as

$$P_{AVE} = Q_{E_TOT} \cdot f_{shots}$$
6-5

Eight shots per minute is used here; $f_{shots} = 8 / 60 = 0.133 \text{ Hz}$.

Table 6-9 Average power dissipation of switches

<i>Device</i>	<i>Power dissipation (W)</i>
CM400HU-24F	20.64 W
CM400DY-66H	36.8 W
It is desirable to mount all of the switches on a single heat sink	
6 × CM400HU-24F	123 W
2 × CM400DY-66H	73.6 W
Total dissipation	≈ 200 W

Table 6-10 Relevant heatsink technologies with natural cooling

<i>Heatsink</i>	<i>Width [mm]</i>	<i>Length [mm]</i>	<i>R_{TH} [°C/W]</i>
Semikron P38	300	500	0.112 (single source)
Semikron P35	200	1000	0.13 (2 – source)

Assuming a $\Delta T_{sa} = 30^{\circ}\text{C}$ and a 200 W dissipation, a thermal resistance of 0.15 is required. The chosen sink is the P35 model; this considerably eases switch bank construction as all the switches need to be mounted onto this single block. The sink is a flat-top mounting block with dimensions ($w \times l \times h$) 200×1000×40 mm.

6.6.2 Snubber design

The sharing method is discussed in section 3.11.3. Eq. 4-48 with $t_{delay} = 1 \mu\text{s}$, $V_{dif} = 100 \text{ V}$, $I_0 = 300 \text{ A}$ gives a required sharing capacitor value of 3μF per device. 2μF capacitors with the required current and voltage rating were available and $C_Q = 2 \times 2 \mu\text{F} = 4 \mu\text{F}$ per 1.2 kV device was used. As a result, $C_{SNUB_{1,3}} = 1.33 \mu\text{F}$.

Snubber capacitors for the 3.3 kV modules are used for precautionary measures only. No sharing is required, soft switching (turn-off snubbing) is not an issue and any load-induced over-voltages will be effectively compensated for by the larger capacitors of Q_1 and Q_3 . However, local loop inductances, modelled as the conduction path T_{SWITCH} , may result in some overshoot. As a result a low-value capacitor is connected across the 3.3 kV modules. Assuming a local loop inductance of 250 NHK (worst-case return path of 25 cm), a capacitor value of 220nF result in a

worst-case overshoot of 320 V (using Eq. C-7). Practically, this overshoot was shown to exist, but is a great deal lower.

Worst-case T_{LOAD} over-voltage compensation is performed using Eq. C-8. A 2 m co-axial cable is used as the load cable. Assuming worst-case conditions, a 4 m return path has an inductance of 4 μ H. This will result in a worst-case overshoot of 520 V for the first transient and then 360 V overshoot for the transients following that (due to effective doubling of the snubber capacitor). For the final system transient – where the system will be at a maximum of 2.4 kV – a superimposed transient of 360 V is still within device ratings. The actual transient is observed to be over-damped, however, indicating that the load inductance is a great deal lower than expected and that the load appreciably dampens the oscillations.

6.6.3 Busbar construction

The busbar construction is of considerable importance, both in the prototype and in the final commissioned system. In order to determine how the devices are to be connected, an analysis is made of the actual flow paths that result during commutation.

Different current flow paths exist during the different stages of conduction. Documented here is the analysis method performed for a single switch transient for Q_3 . The other transient analyses are similar and are not presented. Recognition of the actual current flow paths is important, as the bus structure is not standard; throughout the transients, the currents commute through different and varied paths. It is in our interests to lump these paths so that forward and return paths lie physically close to one another; this reduces stray inductance and EMI problems.

Three specific transient paths are recognised. Each switch transient involves commutation of the full charge current from the switch modules (and connected buswork) to the load. Each module's switch elements are grouped and the local buswork (forward current and return current path) is lumped into a single transmission line element called T_{SWITCH} . Each switching transient commutates through a local buswork structure common to all the modules; this is lumped as T_{LOCAL} . The load path – parasitics in the load cables and in the load itself – is further lumped as T_{LOAD} .

Fig. 6-5 displays the full XRAM topology and indicates the different current flow paths. In unbroken bold is the path where no current change takes place. In dotted bold is the path (forward and return) of T_{LOCAL} , which experiences an I_0

transient superimposed on the initial I_0 . The fine dotted line represents the full T_{SWITCH} current path, where current reduces from I_0 to 0 A. The dot-dash line is the load path, or T_{LOAD} , which also experiences an I_0 transient superimposed on the initial I_0 .

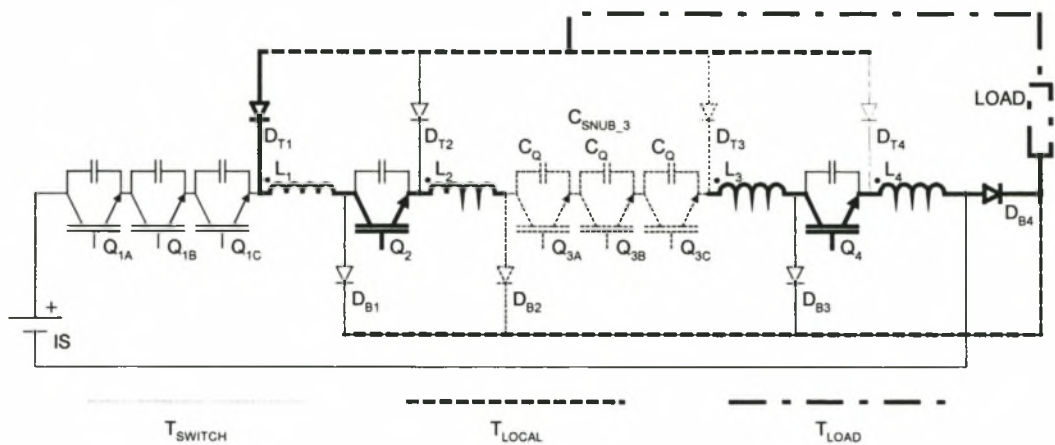


Fig. 6-5 XRAM topology current flow path recognition

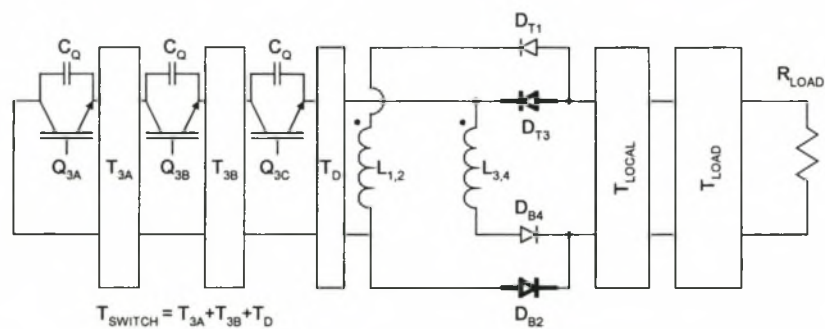


Fig. 6-6 Current flow path model

Fig. 6-6 displays the effective transmission line model of the current flow paths and indicates where in the circuit each component is located.

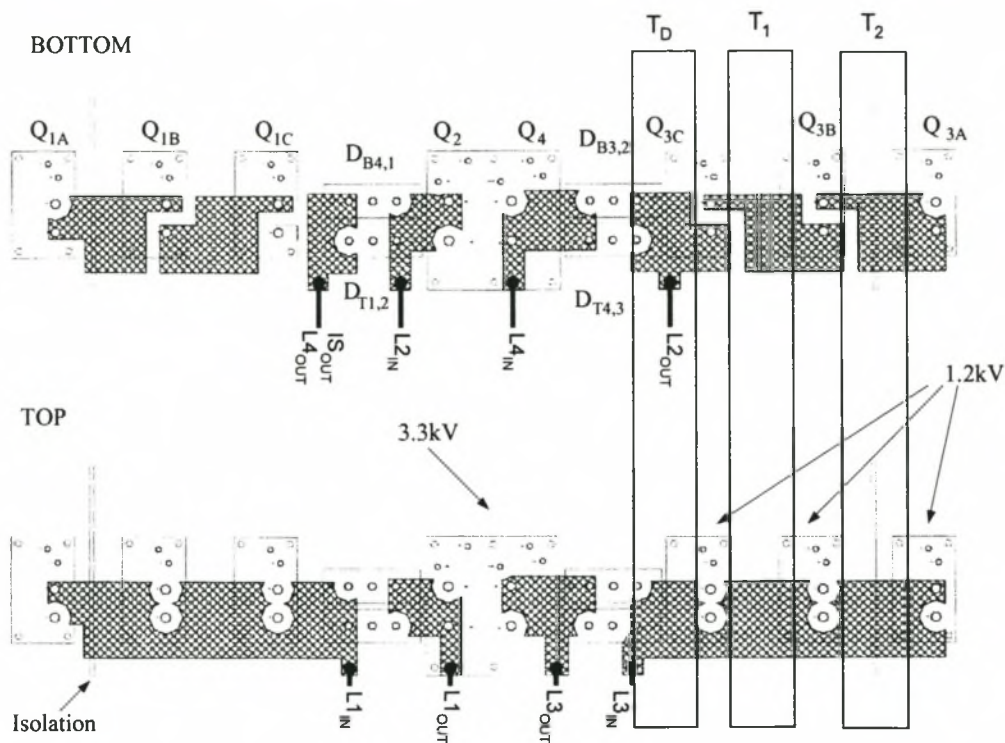


Fig. 6-7 Constructed system current flow paths and device placing

Fig. 6-7 shows the resultant construction method that was employed to reduce – and effectively localise to a recognisable area - T_{SWITCH} . Shown is the current forward (TOP) and current return (BOTTOM) paths of Q_3 and of the relevant diodes that commute during this transient. Hatched areas are isolated bus-plates separated with standard G-11 isolation material. Fig. 6-6 shows schematically where these paths lie. In bold in Fig. 6-6 are the diodes that commute in this transient. The other two (not bold) are conducting and experience no current transient.

Also included in Fig. 6-7 is an isolation marker. The 1.2 kV devices have an isolation voltage rated at 2.5 kV. It is possible that the collector of Q_{3A} and the emitter of Q_{3C} will experience a potential difference of more than 2.5 kV. The third device (Q_{3C}) of the two series switches are placed on their own isolated heatsink. The emitter of this device is connected to the relevant heatsink (this will also reduce the possibility of capacitive coupling between the device driver and the sink). The battery negative terminal is connected to the major sink.

T_{LOCAL} and T_{LOAD} are not shown in Fig. 6-7. T_{LOCAL} takes the form of two raised (15cm) bars, one linking the top diodes (those with prefix T) and one linking the bottom diodes. T_{LOAD} is composed of two meters of coaxial cable (obtained from the AEC) and a low inductance $CuSO_4$ solution load.

6.6.4 Controller design

A custom ATMEL microprocessor-based controller board was developed for the control of the switches. The charge cycle is initiated with the closure of the all the switches. Current feedback is implemented through the use of an appropriate LEM and a comparator is used for level detection. The current feedback signal proved very noisy, but was still useful (a watchdog is placed in the code to circumvent sensor failure). The IGBTs were discrete and required custom-built isolated supplies. Control is performed through the use of optical fibres. Control software failure was not considered. A standard boot-up / control hardware failure hardware check is also installed, which switches all the switches *ON* except for Q_1 . This could be altered by way of jumpers. The controller board is physically removed from the system to avoid possible EMI problems.

6.7 System results

This section documents system results incorporating load and source current and voltage waveforms. It is in the interests of the designer to validate the expected (simulated) outputs with measured values. Of interest is the source current magnitude, transient curves and total charge time. On the load side, load currents, load voltages and discharge variability are of interest (at the required power levels). Individual switch transient simulations are performed using Matlab. System simulations are performed using Spice.

6.7.1 Source current

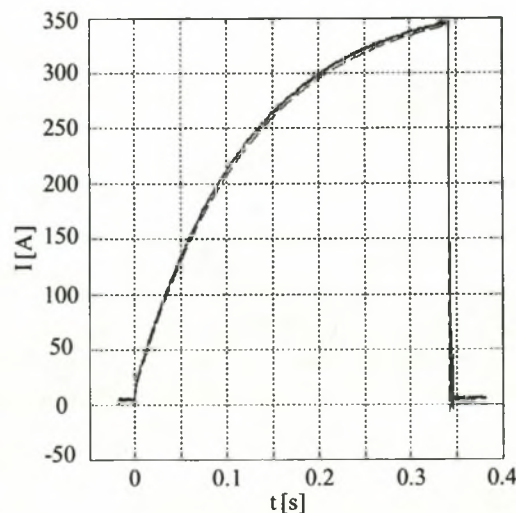


Fig. 6-8 IS current measured and simulated

The measured and simulated values of Fig. 6-8 are in good agreement (the simulated values are in this case generated using spice). Two important modifications were applied to the model. Firstly, the specified IS_{ESR} was measured to be higher than specified in the data sheets. For this measurement, the batteries exhibited a voltage of 111.8 V, which translates to an energy capacity of 60% [81]. This increase in ESR is of distinct interest to the designer; this is reconsidered in the closing chapter. Analysis of Fig. 6-11 calculates an ESR per battery of 6 m Ω , as opposed to 3.5 m Ω specified by the data sheets (actually calculated from expected voltage drops for set current levels). The coupling factor is held at 0.96 (measured) and each inductor self-inductance at 2 mH (measured). The resulting simulation closely matches the measured values.

6.7.2 Load discharge waveforms

The two outputs of interest are the load power levels achievable, load power waveforms and delivered energy waveforms.

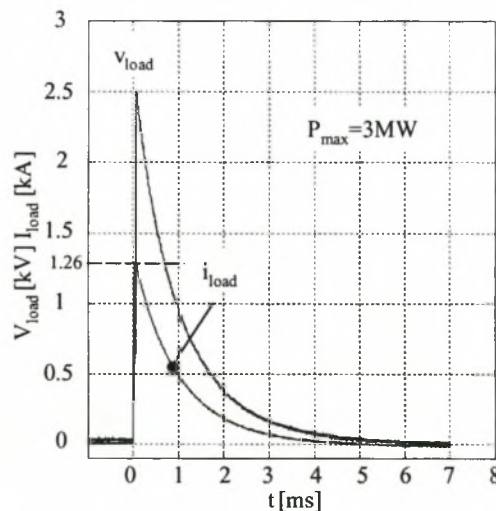


Fig. 6-9 Measured load voltage and current at full ratings

Variation of the discharge power is determined by the value of the load resistor and firing delay time. Fig. 6-9 shows a peak power output of just over 3 MW using a 2 Ω load. Fig. 6-10 shows the voltage and energy discharge profiles for three different discharge schemes (each utilises different switching times of the relevant modules). Of interest to the designer is the extended discharge time that is possible, the lower power levels possible and the variation in energy discharge possible. The full inductor is a 32 mH device conducting approximately 330 A. This translates to a

stored energy of 1 720 J. The total back-end transfer efficiency of the three profiles calculates to 93%, 92% and 86%. However, the use of inductor modularity clearly allows for a controlled energy transfer rate.

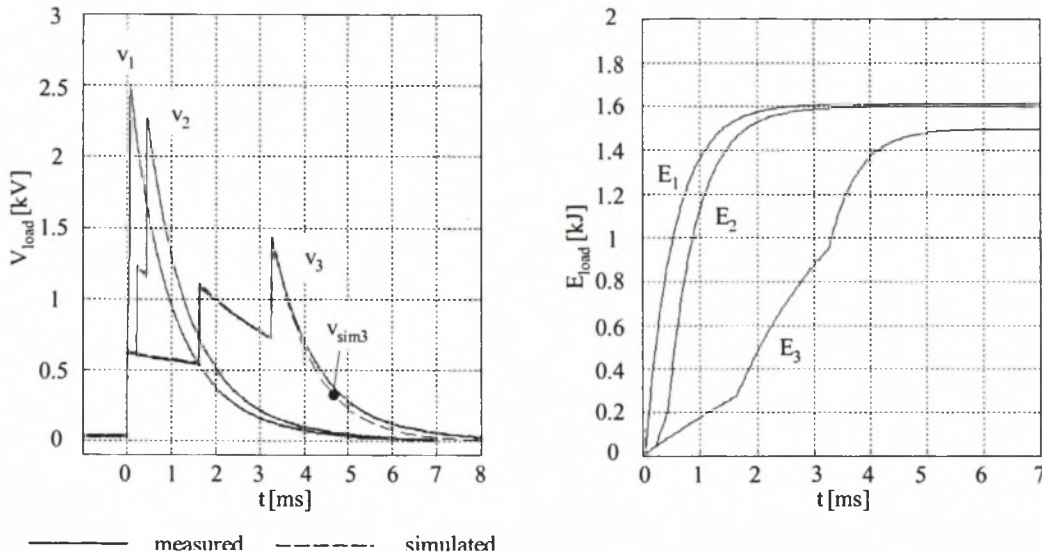


Fig. 6-10 Output voltage and energy for 3 different discharge profiles

The switching times for these measurements were all synchronous with delays of 30 μ s, 200 μ s and 1600 μ s respectively, with a 6 μ s delay between Q_2 and Q_4 .

6.7.3 IS results

Of interest to the designer concerning the IS is the nature of IS_{ESR} during the charge phase. The design model assumes a constant IS_{ESR} throughout the charge cycle, at a known value. Analysis of Fig. 6-11 shows that IS_{ESR} does indeed remain constant throughout the charge cycle, although the current is not near the devices rated short circuit current of 2 500A. However, it is observed that the IS_{ESR} value of 54 m Ω translates to 6 m Ω per battery, which is higher than the specified value. This is because the battery is not at full charge; reference to [81] shows that the battery is near 60% charged. Such a dependency is important if IS_{ESR} is used as a design variable in the system optimisation protocol discussed in Chapter 4.

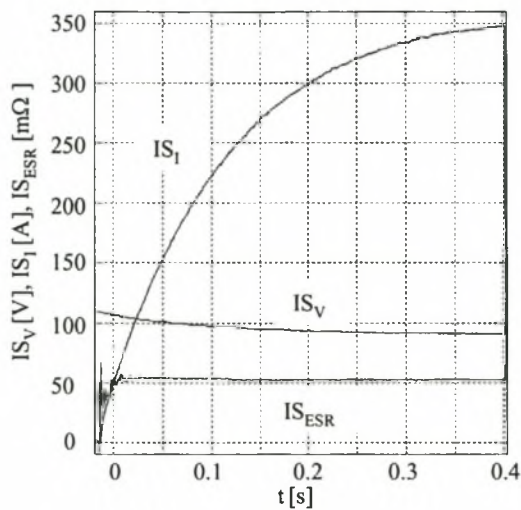


Fig. 6-11 IS characteristics during charge cycle

6.7.4 Load results

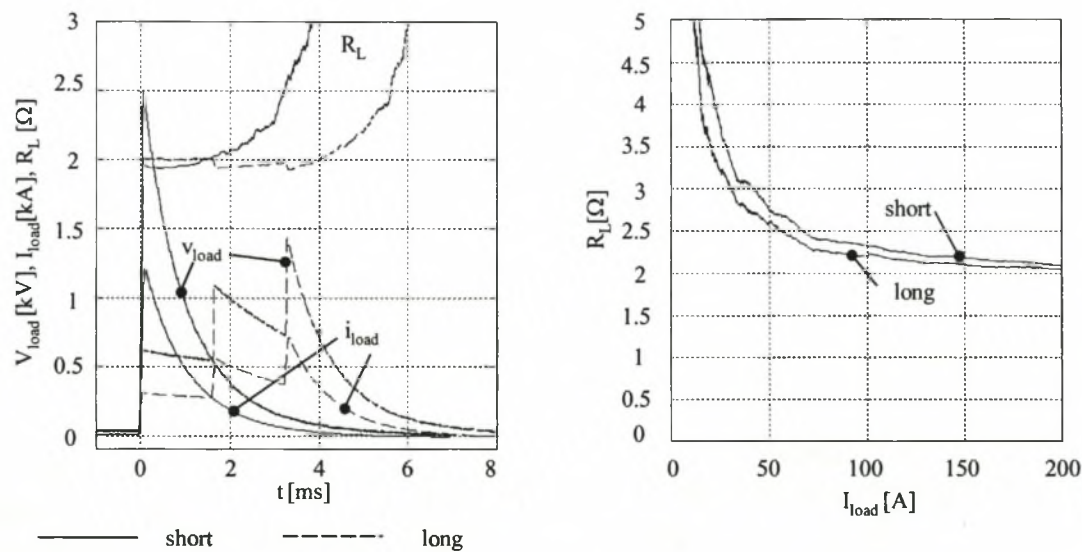


Fig. 6-12 Load characteristics during discharge cycle

Modelling of a salt-solution load is subject to so many parameters that the empirical approach used here is considered the best. It is observed that from Fig. 6-12 that the resistance is dependent on the load current, particularly at low currents. The long resistance reference is to the large charge time step trace of the left-hand side graph and the short refers to the other.

This has little effect on the testing of the circuit, however, and is included for the sake of completeness. It is observed that the load resistance changes as a function

of the load current; exact load value prediction is not required and the average value at high current, shown at 2 Ω , is sufficient.

6.7.5 Switch voltage sharing results

Switches Q_1 and Q_3 are composed of three serially connected 1.2 kV devices. Capacitive sharing across the devices has been implemented.

Fig. 6-13 shows the voltage sharing across the three devices. As observed, the sharing is effective in providing for a maximum voltage difference of 40 V. Superimposed on this voltage (when the devices are switched) is the IS voltage.

Fig. 6-14 shows the voltage sharing across the three devices of Q_3 . The maximum voltage difference – for the full load voltage of 2500 V – is 15 V.

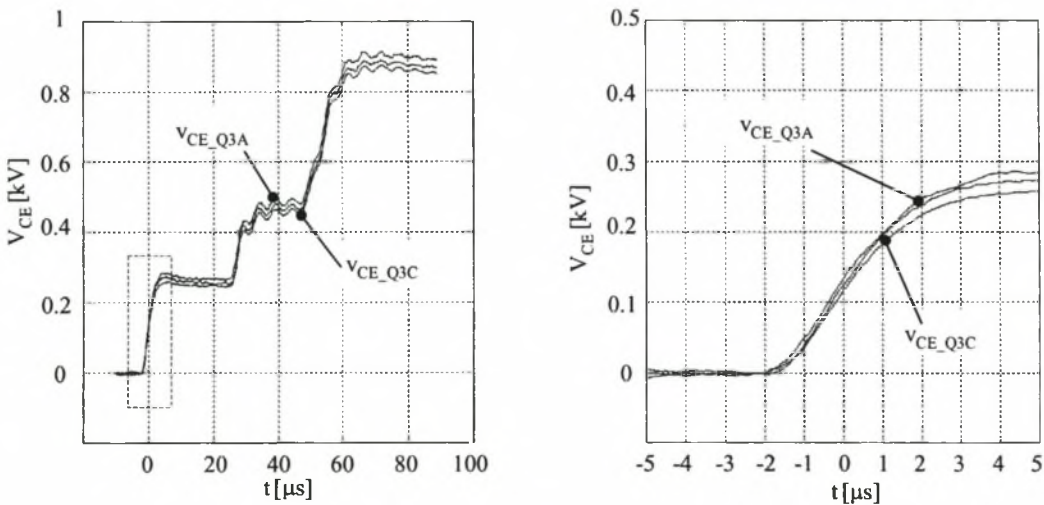


Fig. 6-13 Switch Q_1 voltage sharing

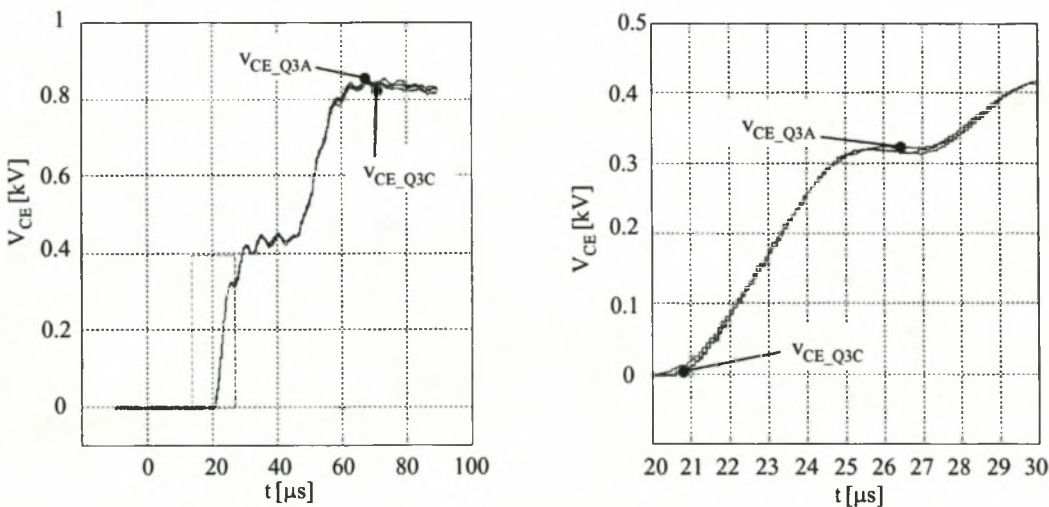


Fig. 6-14 Switch Q_3 voltage sharing

6.7.6 Switch commutation waveforms

Of interest to the designer are the voltage and current transients that occur in each switch module. Each transient occurs in a switch group including the opening switch (the IGBT), the two freewheel diodes and the snubber capacitance, composed of the snubber capacitance of the current switching module and all the already switched modules, or the C_{COM} of section 3.5. The switching transient follows a path as documented in section 3.5.

It is assumed that the IGBT switches instantaneously and that during the transient, the inductors current remains constant. When switched, the conduction current is passed to the device's snubber capacitor. The voltage will rise linearly until the diodes in the module freewheel path commute. From this point on the load appears as resistor in parallel with the compound snubber capacitor; current commutates through the diodes, reduces through the capacitor and increases in the load.

The readings shown here show voltages across the IGBT, the sum of the voltages across the relevant diodes and the switch current; current commuting out of the switch is the same as that commuting into the load. The load current is thus processed to represent the switch current for each transient. The load current is, however, only representative of the switch current around the switch cycle, and must be ignored for all other times for each graph.

Switch Q_1 commutation transient

Fig. 6-15 displays the relevant switch transients for switch Q_1 (measured from the emitter of Q_{1C} to the collector of Q_{1A}). Shown is the switch voltage for all the switching transients. The device current shown is measured at the load and is valid (in this instance) only before the switch transient till just before the next switch transient.

The diode voltage measured is the sum of the designated diode voltages. The initial voltage level of 108V confirms the bias-point analysis performed in section 3.4. It is observed in the close-up that a small voltage bump occurs on V_{CE_Q1} and on the diode voltage. This phenomenon is better displayed in Fig. 6-18. The simulations are performed using the model of 3.5 with the following parameters: $C_{snub_I} = 1.33 \mu\text{F}$, $C_{COM} = 1.33 \mu\text{F}$, $R_L = 2 \Omega$, $I_{Q1} = 330 \text{ A}$, $I_{IN1} = 108 \text{ V}$.

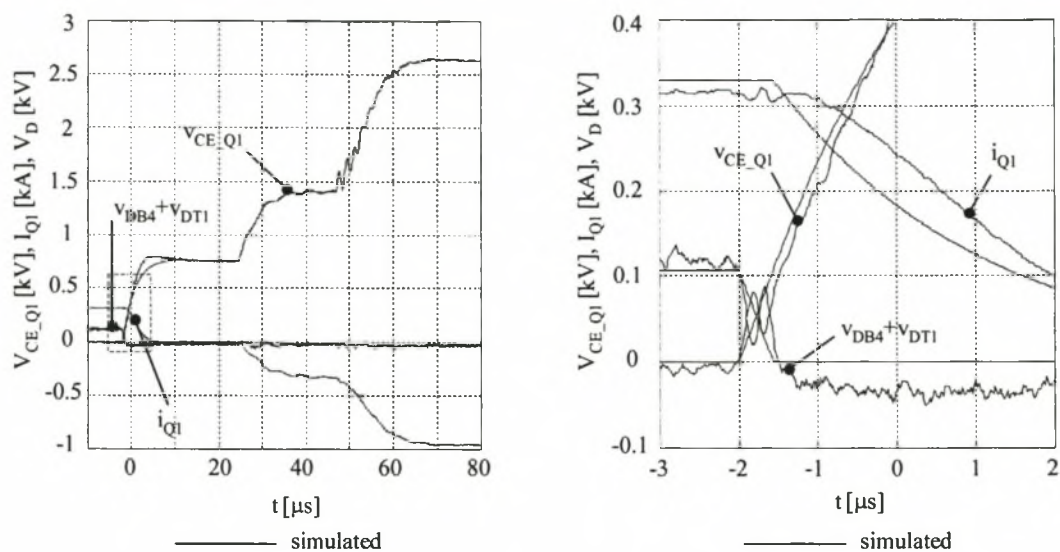


Fig. 6-15 Switch transients for Q_1

It is observed that there is fair agreement for the diode and IGBT voltage; the transient is too short to obtain accurate comparative results. Better correlation is observed in the other transients. V_{CE_Q1} exhibits a peak, which is not modelled. This is a direct result of the load inductance (it is observed that the current also takes longer to commute than expected), which is not included in the transient model.

Switch Q_3 commutation

Fig. 6-16 shows the switching transients of switch Q_3 . Switch Q_3 is switched for switch cycle 2; this is performed to enforce balanced discharge. The measured quantities are analogous to those of the first switch cycle. It is observed that the simulations more accurately match the measured data; in this case the snubber capacitor controls the voltage rise during most of the transient and as a result the model is valid for a longer period. The simulations are performed using the model of section 3.5 with the following parameters: $C_{snub_3} = 1.33 \mu F$, $C_{COM} = 2.66 \mu F$, $R_L = 2 \Omega$, $I_{Q1} = 320 A$, $I_{IN1} = 640 V$.

It is observed that the effect of the load inductance is substantially reduced; the increased compound snubber capacitance mitigates its effect to a great degree, although one might expect to see a more pronounced effect.

Of interest here is the measured high-frequency ripple that is superimposed on the major transient. This ripple is also observed (to a lesser degree) on the load, which indicates that the load inductance is lower than expected and that the load assists in

damping the oscillations. This ripple effect will only occur for this and the following transients.

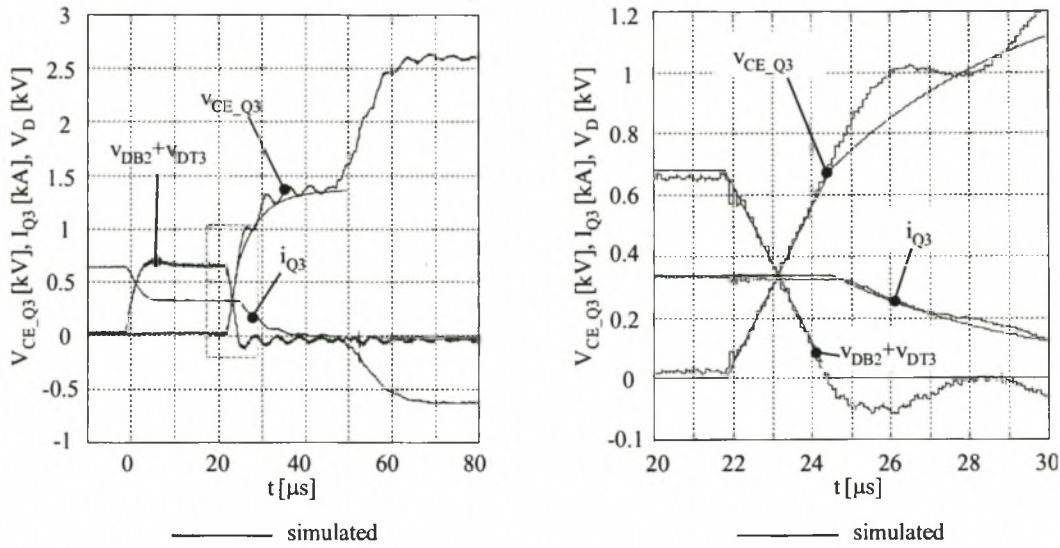


Fig. 6-16 Switch transients for Q_3

However, analysis of the waveforms shows that if the oscillation is due to a local loop inductance its value must be over 30 μH (calculated from the graph). This high value is very unlikely. It is shown in section 6.7.7 that the likely cause of these oscillations is the stray capacitance of the inductor source.

Switch Q_2 commutation

Fig. 6-17 shows the transients of switch cycle 3, or the switching transients for Q_2 . The description of this switch transient is analogous to that of the preceding sections and is not repeated. The simulations are performed using the model of section 3.5 with the following parameters: $C_{snub_2} = 220 \text{ nF}$, $C_{COM} = 2.88 \text{ }\mu\text{F}$, $R_L = 2 \text{ }\Omega$, $I_{Q1} = 300 \text{ A}$, $I_{JN1} = 1270 \text{ V}$.

This transient model is only valid for 6 μs , up to 52 μs . After this, Q_4 switches and the transients change. However, it is observed that the simulations are in good agreement with the results.

Of interest again are the high-frequency oscillations observed on V_{CE_Q2} . As these oscillations are also observed across Q_1 , it is unlikely that it is the result of only the module local loop inductances as if this were the case they should only occur across Q_2 .

Of interest to the designer is the fact that no over-voltages or unpredicted diode commutation will result and that the load wave-shape is not corrupted (which from measurement we observe it is not). The IGBTs do not experience over-voltages. However, the individual diodes may experience over-voltages; this is discussed in section 6.7.7.

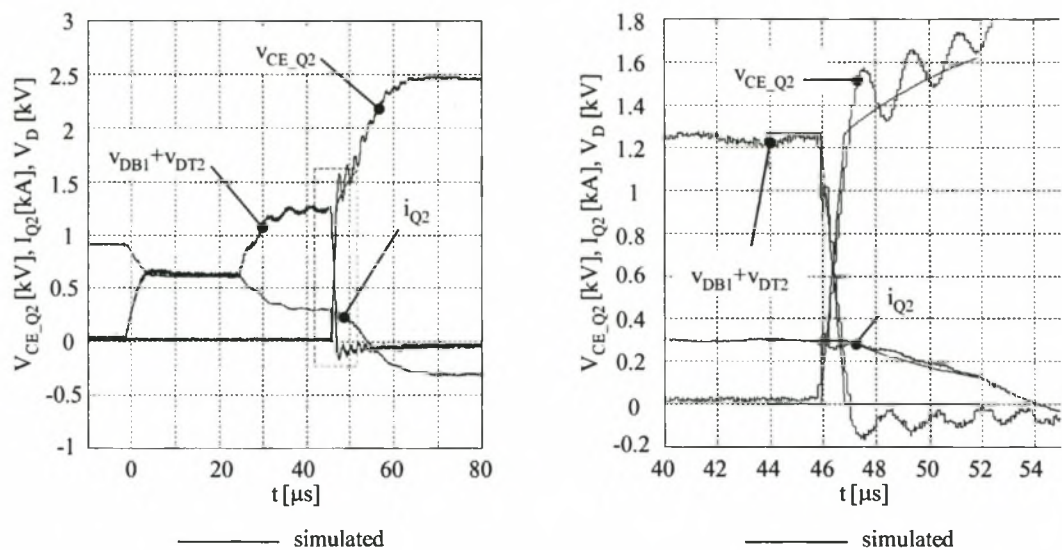


Fig. 6-17 Switch transients for Q_2

Switch Q_4 commutation

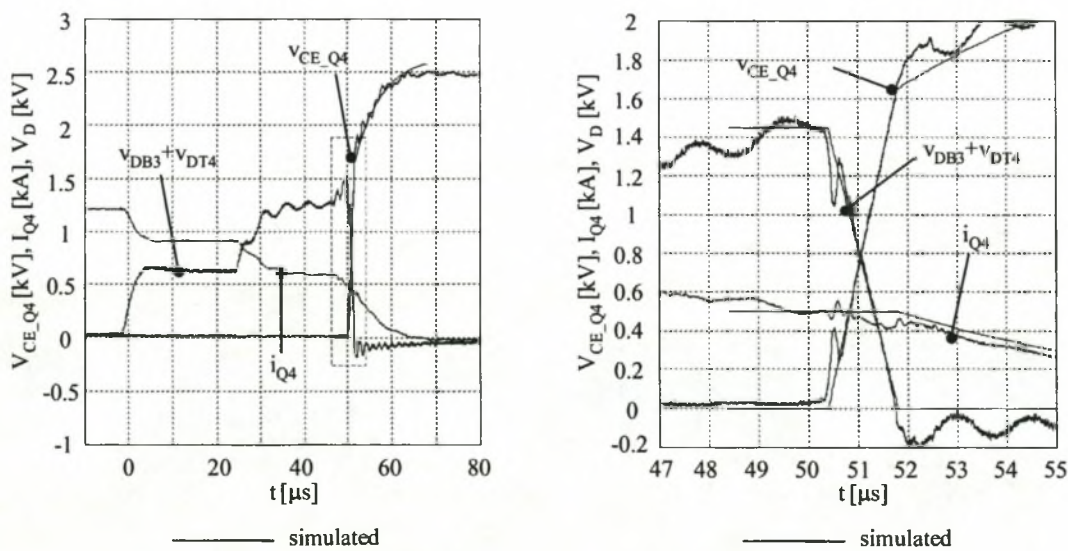


Fig. 6-18 Switch transients for Q_4

Fig. 6-18 shows the switching transients of switch cycle 4 and of switch module Q_4 . The description of this switch transient is analogous to that of the preceding sections

with one important difference. Section 3.7 discusses the issue of timing for the switching of Q_4 . The issue is that for a coupled and balanced system, the third switch configuration results in unbalanced inductor discharge. As a result, energy transfer between modules takes place and the current of inductors L_1 and L_2 drops faster than that of the still linked L_3+L_4 . It is in the designer's interest to limit this imbalance. Although this phenomenon is not verified experimentally, measured results documented in Fig. 3-6, where a comparable effect is modelled and measured, imply that the system modelling is accurate. Using an allowed imbalance of 20% (defined in section 3.7), and the measured system variables of $R_L = 2 \Omega$, $L = 2 \text{ mH}$ and $k = 0.96$, stage 4 must be switched within $5.4 \mu\text{s}$. $6 \mu\text{s}$ delay is used in this test-run. However, this short switch delay is faster than the other system transients; switch cycle 3 is still busy. Effectively, this results in a relatively complex discharge path. This phenomenon is not modelled other than to state that no instabilities occur during this time; the diodes of switch cycle 3 have already commutated, but the compound snubber capacitor has not reached steady-state voltage. Modelling the load as a parallel connection of the snubber capacitors and the actual load resistor shows that, while there is some energy-interchange on the load side during this phenomenon, no unstable situations can develop at the source side, composed of the storage inductors and the switches, as it has effectively completed commutation in the first $2 \mu\text{s}$ (refer to Fig. 6-17).

The switching model also undergoes a minor change. Due to the persistence of switch cycle 3, the load voltage is actually changing during the commutation of Q_4 . Thus the diode's starting voltage and the switch's ending voltage (signifying the end of the commutation time) will differ. During this stage the diodes are not yet commutated and V_{CE_Q4} rises linearly; it will rise until it matches the load voltage. There are no important ramifications of this small model difference and it has been incorporated in the simulated trace of Fig. 6-18.

6.7.7 Diode voltage consideration

Only the relevant diodes of switch group 4 – diodes D_{T4} and D_{B3} – are considered. The effect is also applicable to the other diode groups.

Shown in Fig. 6-19 is the voltage across diodes D_{T4} and D_{B3} and the sum of the two. Fig. 6-18 uses the sum for switch transient analysis purposes. It is observed

that while the sum of the voltages is predictable – and thus controllable – the individual diode voltage is unpredictable.

Analysis of Fig. 3-12 for the four transients shows the origin of these oscillations. Analysis of switch cycle 1 (Fig. 3-12(a)) shows that diodes D_{T4} and D_{B3} are effectively in series (Q_4 is conducting). The series connection is in parallel to the load, which acts as a voltage level clamp. Average voltage levels are apparent; the voltage loop $D_{T1} - L_1 - L_2 - L_3 - D_{T4} - D_{T1}$, where D_{T1} is conducting and $v_{L1} = v_{L2} = v_{L3} = v_{L4}$, shows that one would expect a voltage of $\frac{3}{4}v_{load}$ across D_{T4} . Likewise with voltage loop $D_{B4} - L_4 - D_{B3} - D_{B4}$, where D_{B4} is conducting, D_{T3} will have a voltage of $\frac{1}{4}v_{load}$. Reference to Fig. 6-19 shows that these average values are correct.

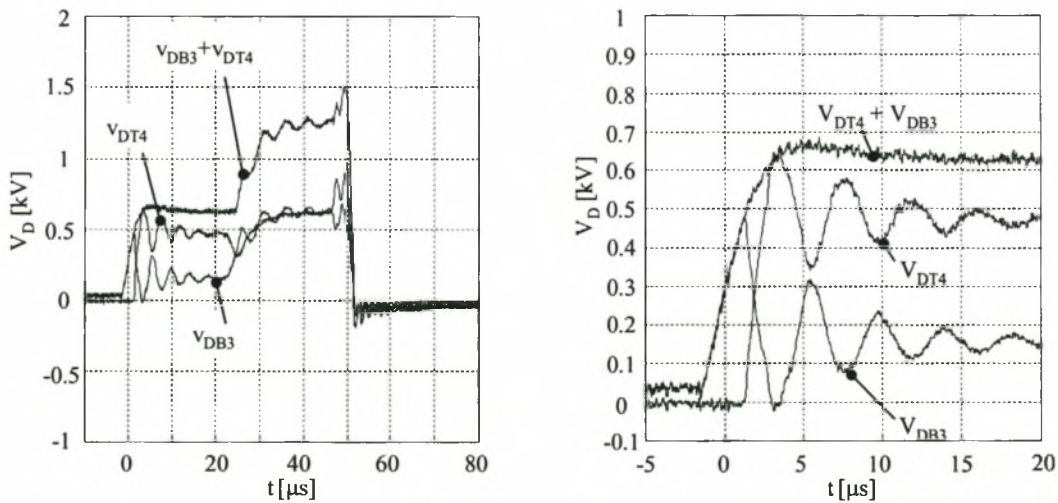


Fig. 6-19 Diode voltage comparisons

However, it is observed from Fig. 6-19 that large voltage oscillations occur across the diodes. In the close-up on the right of Fig. 6-19, it appears that V_{B3} experiences an initial condition and that when D_{T4} turns off, the two voltages somehow resonate. The initial condition observed with the diodes is explained in section 3.7 and in Appendix A. It is the result of the initial current imbalance during the charge cycle; during the current imbalance, D_{T4} is conducting current and is necessarily on. This leaves only D_{B3} to hold the full commutation voltage. Use of Eq. A-8 predicts a current imbalance convergence time for this condition at 1.5 μs . It is measured at 2.5 μs . The close agreement of these results lends credibility to the argument.

It is unlikely, however, that the resulting resonance is the result of the terminal capacitances of the diodes as the resonance frequency is low. The inductor voltages during this time-span are given in Fig. 6-20. It is observed that the current imbalance convergence results in relatively high negative voltages experienced by inductors L_2 and L_3 ; this is also predicted in section 3.7 and in Appendix A.

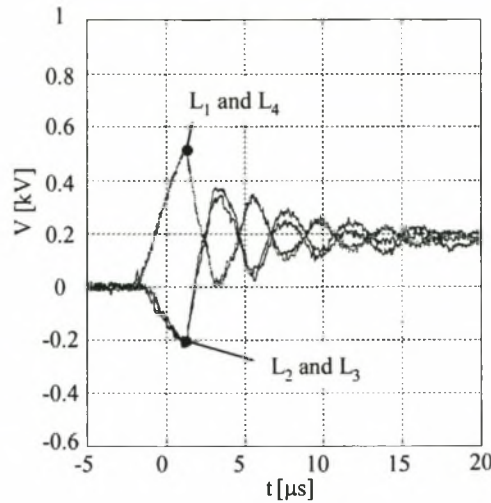


Fig. 6-20 Measured inductor voltages

Unexpectedly, however, the inductor voltages exhibit this same voltage resonance. An ideal inductor can experience a discontinuous voltage step; ideally, the voltages of Fig. 6-20 should experience the initial transient but then snap to the steady-state values when diode D_{T4} starts conducting (this is demonstrated in the simulation of Fig. 6-21).

Some unmodelled capacitance in parallel with the inductor causes this resonance.

The inter-winding capacitance of the inductor is roughly calculated. With a conductor length of 500 m, a conductor width of 1 cm and an inter-conductor distance of 0.5 cm and assuming that two sides of each conductor play a role in the capacitance, the total inductor capacitance is calculated as

$$L_{CAP} = \epsilon_0 \frac{A}{d} = \epsilon_0 \frac{500 \cdot 0.01}{0.005} = 9nF. \quad 6-6$$

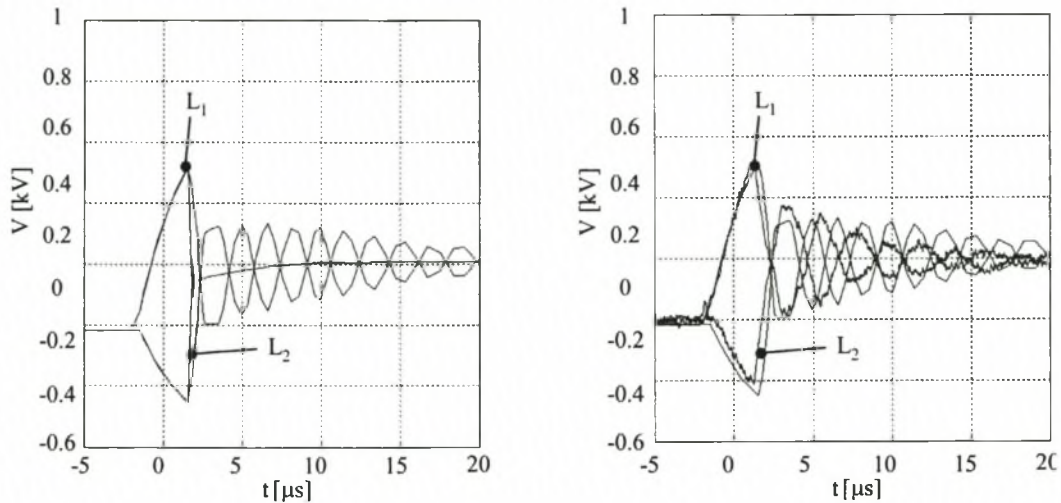


Fig. 6-21 Simulated and measured resonance of inductor capacitance

Simulation using spice and simply connecting a capacitance of 2.5 nF across each inductor gives inductor voltages shown Fig. 6-21.

On the left of Fig. 6-21 is the simulated inductor voltages for the ideal case (zero capacitance) and the derived case. It is observed that the inclusion of this capacitance alone results in large oscillations. Comparison of the right-hand graph of Fig. 6-21 of measured and simulated waveforms are in remarkable agreement considering the crudeness of the simulation.

Examination of Fig. 6-19 shows that when the last two switch stages occur (this is just before the diode voltages fall to zero on the left-hand graph of Fig. 6-19), oscillations occur that increase the diode voltage above that expected; this could result in diode over-voltages and device failure. Examination of Fig. 3-12(c) shows that during this transient, an unbalanced discharge is also occurring. The phenomenon appears to be related to this occurrence.

It is assumed that inclusion of capacitors across the diodes will reduce the magnitude of the oscillations (according to Eq. C-7). This method of over-voltage mitigation is not verified experimentally, however.

6.8 Summary

It is apparent that the volume models are limited in predicting valid practical systems. This is due to the fact that the sub-systems are not continuous functions of volume. This situation will only occur if the system is of low energy or if the battery technology used has a high specific power, however. For large energy systems the continuous model will make more accurate predictions.

A modification of the discrete model is presented that circumvents this requirement of continuous elements and allows for practical volume calculation. It should be kept in mind that this model is originally derived from the discrete model which – in its simplest form – provides identical results to those of the continuous model and that proposed by Soreq.

An example of the design algorithms outputs is given (in Fig. 6-1) and a table comparing the effect of the system modifications of, in particular, the inclusion of Q_{v_on} is also included. Its effect is shown to be appreciable.

Various applicable construction considerations and details are given.

Relevant results are shown, documenting the necessary electrical stability concerns discussed in the previous chapter. The list of important results are as follows:

1. It is observed that the series connection of IGBTs is possible.
2. All the discharge modes are presented.
3. Current imbalance measurements and predictions are shown to agree.
4. Stray inductances are shown to be minimal and not of too great a concern.
5. Stray capacitance is shown to of concern as regards the voltage ratings of the diodes.
6. The system is operated at full power.
7. An example is giving showing the variable energy transfer pulse shapes possible.

The system has matched all required specifications. These can be listed as follows:

1. The use of semiconductor switches (although underrated) in long charge time inductor-based PFNs is validated.
2. The use of a coupled modular storage element (and value prediction) is validated.
3. The volume algorithm proposed in the preceding chapters is validated.
4. The transients and switching behaviours are all stable and predictable.
5. Pulse shaping is performed using delayed switching of the modules.
6. The required 2.5 kV and 1.2 kA voltage and current levels were achieved, resulting in a 3 MW controllable output pulse.

The prototype is used to demonstrate that a modular, inductive storage, volume-optimised system can be constructed according to definable volume and electrical

models. Although scaling of the system is a definite issue, it is proved – in principle – that the algorithms discussed and proved in this report are correct.

CHAPTER 7

PWM OF AN INDUCTIVE STORAGE PFN

7.1 Introduction

7.1.1 What is pulse width modulation?

Pulse width modulation (PWM) of a signal generally involves the approximation of a waveform through a train of discrete pulses, where the width of each pulse is tailored so that the effective average of the train matches the desired waveform. Application of such a scheme for millisecond pulse forming is only made possible through the use of fast switches, so that the resulting switch transients do not adversely affect the required output pulse shape and the switching losses do not become excessive.

7.1.2 What advantages can be gained through PWM?

According to section 3.3, the full system volume is independent of module number. This implies that any output pulse shape is achievable. However, section 3.3 shows that the usable switch states (that is, the output levels available for pulse forming) is related to the module number by the relation

$$n = 2^{\text{states}-1}. \quad 7-1$$

Thus, as the required pulse shaping increases in complexity, the required module number increases with an exponential relation.

However, this is limited practically as an increase in module number will invariably result in increased peripheral system requirements (additional bus-structures, interconnections and sub-system complexity) and cannot go on indefinitely. Thus it is still in the designer's interest to keep the module number to a minimum.

PWM of the output pulse shape will allow improved control of the rate of energy transfer to the load over a non-PWM modular system. This chapter demonstrates accurate pulse forming with the use of only two modules.

7.1.3 What are the relevant issues behind PWM?

When PWM is used in an inductive storage millisecond PFN, the actual storage inductor switches from a combined series discharge state to a parallel discharge state and then back again, as demonstrated in Fig. 7-. Fig. 7-(a) shows the equivalent circuit and the active elements. Fig. 7-(b)-(d) shows the progression of the different switching states and Fig. 7-(e) and (f) shows the resultant power and energy transfer wave-shapes.

During switching (both on and off), it is of interest to note the electric stresses placed on the switch itself, discussed in the next section, and the effect of balancing of the inductor currents, discussed in Appendix E.

Through the correct sequential timing of these discharge states, it is possible to match a required power or energy discharge wave shape. These control issues are discussed in section 7.3.

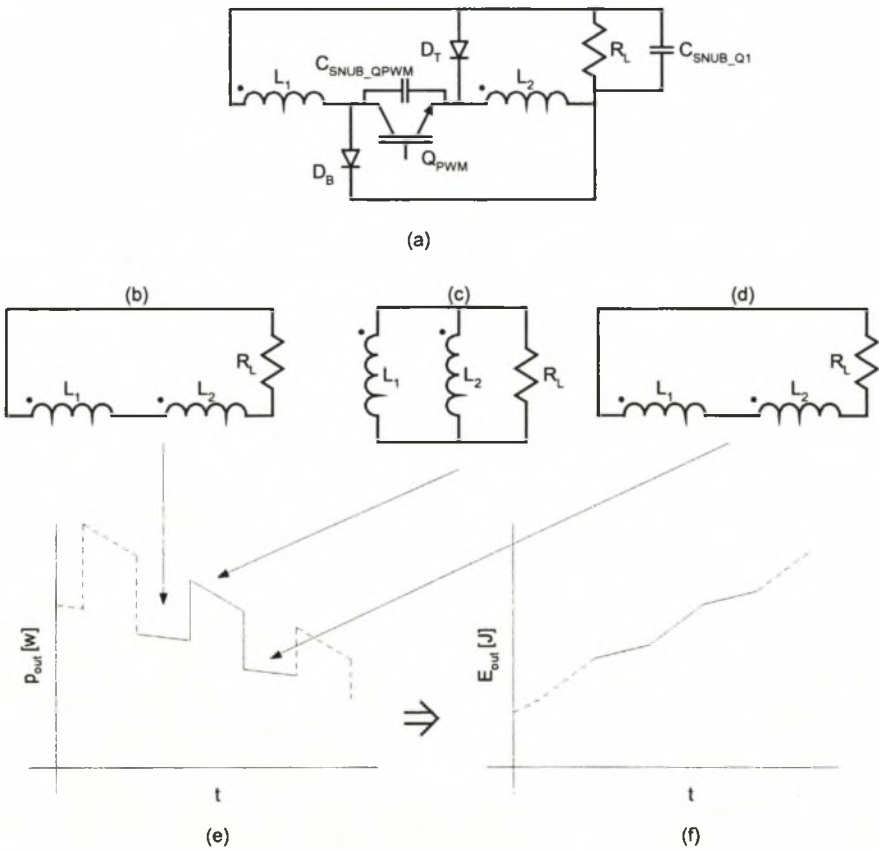


Fig. 7-1 PWM circuit equivalent

7.2 Switch waveforms

The transient between the states of Fig. 7- (b) and (c) (turn off) is the same as that discussed in section 3.5. To briefly recapitulate with reference to Fig. 7-, the switch is modelled as a linearly decreasing current source. While commutating, current is passed to its snubber capacitor $C_{SNUB_Q_{PWM}}$ and the combination of these two elements determines the voltage rise $V_{CE_Q_{PWM}}$. When equal to V_{RL} , the diodes D_B and D_T are forward biased and current commutation into the load commences. As Q_1 (not shown in Fig. 7-) has already switched, its snubber capacitor $C_{SNUB_Q_1}$ and that of Q_{PWM} , $C_{SNUB_Q_{PWM}}$, combine to form the compound capacitor of section 3.5, which assists in shaping the commutation transient.

It is observed that for a worst-case approximation, the switch is subject to waveforms associated with an inductive load with no snubbing. Other effects concerned with this transient – such as inductor imbalances – are not of immediate importance; they are dealt with in Chapter 3 and Appendix F and not repeated.

The turn-on switch cycle has not been considered yet and is presented here. This is the transient that occurs between the states of Fig. 7-(c) and (d).

The switch Q_{PWM} is modelled as a linearly decreasing voltage source during its turn-on cycle. Fig. 7-2(a) shows the switching waveforms assuming that the load is only resistive and no snubber circuitry is involved. As Q_{PWM} commutates (and defines its voltage drop), current commutates through the switch in a linearly increasing fashion and similarly decreases in the diodes. When the diode current reaches zero, the diodes are reverse biased and Fig. 7-(d) represents the system. From this time on, the load appears inductive and the waveforms are as shown. If the snubber capacitor is included in the consideration, the waveforms appear as shown in Fig. 7-2(b). The time t_{on} is the same for both cases Fig. 7-2(a) and Fig. 7-2(b) as it is defined by the switch

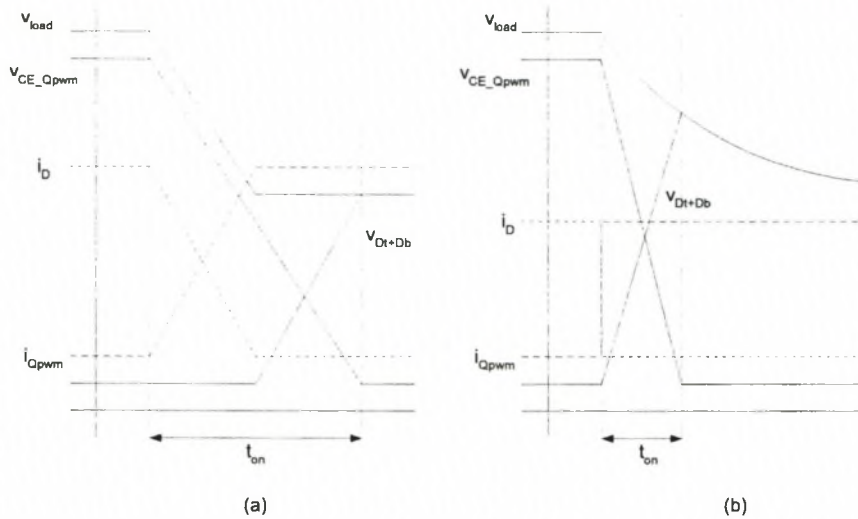


Fig. 7-2 Switch waveforms

alone; if a capacitor-only snubber is used for Q_{PWM} , then the energy stored in the capacitor will necessarily be dissipated in the switch. Other snubber methods can prevent this. The compound snubber of section 3.5 is at this stage composed only of C_{SNUB_Q1} . If the time constant $R_L C_{SNUB_Q1}$ is appreciably larger than the switching time t_{on} , the load can be viewed as a ‘stiff’ voltage and the switching waveforms will appear as if the load is inductive and the switch is switched hard. Thus at the moment of commutation, the diode pair will snap off; current will immediately conduct through Q_{PWM} and the voltage rise across the diode will equal $V_{load} - V_{CE_QPWM}$.

Of importance is the diode voltage that occurs at this stage. It is observed that the combined diode voltage can possibly reach the switch’s off-state voltage (as opposed to half this value as determined in Fig. 7-2(a)).

It is shown in Appendix E that, if a current imbalance occurs during the parallel discharge state, which is probable, then the current imbalance must converge to zero before the stage of Fig. 7-(d) exists. The current imbalance is small and its effect on the source to load energy transfer is negligible. However, while it persists it will force one of the diode pair to conduct. This means the other diode must hold the full voltage during turn-on of the switch. Thus the diodes must have a voltage rating equal to the switch.

For the prototype used in a two-module configuration, $L = 8$ mH and $M = 7.68$ mH and for $R_L = 1$ Ω , the expected time of convergence for a 5% current difference (where $I_{REF} = 1.05$) equals 16 μ s. The 3.3 kV switch is used as Q_{PWM} , which means

that $t_{on} = 1 \mu s$. The load side time constant taking $C_{SNUB_Q1} = 1.33 \mu F$ into account is equal to $1.33 \mu s$. Although the load side time constant is fast, a worst-case assumption can be made that a single diode may have to hold the full load voltage when the load is at its highest voltage value. This limits the load voltage for this research to 1.2 kV.

7.3 Synchronous open loop control strategy

It is assumed that the discharge states can be modelled as constant voltage values (as opposed to exponential decay) as shown in Fig. 7-3.

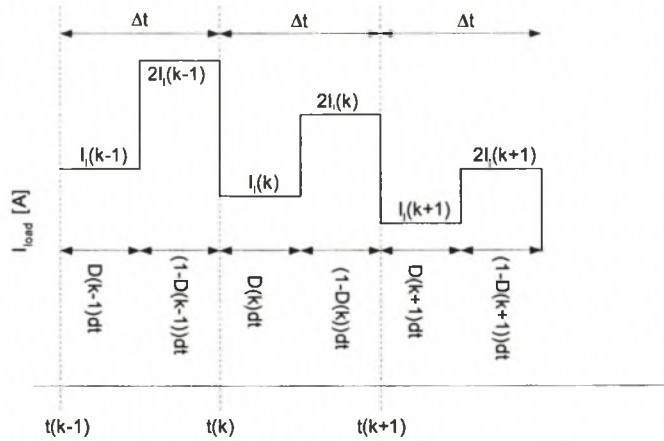


Fig. 7-3 Decay approximation

The control strategy can be described as synchronous as the period time Δt of Fig. 7-3 is held constant. The duty cycle D is less than one and the inductor current level I_l changes for each period. It is clear that the above waveform can be written as a difference equation. The instantaneous power level $P(k)$ at the load at the time $t(k)$ equals $P(k) = R_L I_{load}^2(k)$.

For the time period $t(k) < t < t(k) + D(k)\Delta t$,

$$\begin{aligned} I_{load}(k)_{D(k)} &= I_l(k) \\ P(k)_{D(k)} &= R_L I_l^2(k) D(k) \quad , \\ E(k)_{D(k)} &= R_L I_l^2(k) D(k) dt \end{aligned} \quad 7-2$$

and for the time $t(k) + D(k)\Delta t < t < t(k) + (1 - D(k))\Delta t$,

$$\begin{aligned} I_{load}(k)_{1-D(k)} &= 2I_l(k) \\ P(k)_{1-D(k)} &= R_L 4I_l^2(k) (1 - D(k)) \quad . \\ E(k)_{1-D(k)} &= R_L 4I_l^2(k) (1 - D(k)) \Delta t \end{aligned} \quad 7-3$$

The average load power $P_{AVE}(k)$ for the time interval Δt starting at $t(k)$ is given as

$$P_{AVE}(k) = \frac{E(k)_{D(k)} + E(k)_{1-D(k)}}{\Delta t}, \quad 7-4$$

which equals

$$P_{AVE}(k) = R_L I_L^2(k)(4 - 3D(k)). \quad 7-5$$

It is required to determine the required duty cycle $D(k)$ (the output function) from the given $P_{AVE}(k)$ (the input function) and measured or calculated $I_L(k)$.

It is clear that some feedback is required in the form of $I_L(k)$. As no feedback is used in this example, it is necessary to predict this value. This is performed through the use of the energy stored vs. energy dissipated equation. The instantaneous energy stored at time $t(k)$ equals

$$E(k) = \frac{1}{2} L_{ST} I_L^2(k). \quad 7-6$$

The energy transferred to the load in the time duration Δt starting at $t(k)$ equals $P_{AVE}(k)\Delta t$, which equals

$$E_{transferred}(k) = (R_L I_L^2(k)(4 - 3D(k)))\Delta t. \quad 7-7$$

The instantaneous energy at time $t(k+1)$ is thus equal to

$$E(k+1) = \frac{1}{2} L_{ST} I_L^2(k+1) = \frac{1}{2} L_{ST} I_L^2(k) - (R_L I_L^2(k)(4 - 3D(k)))\Delta t, \quad 7-8$$

which can be rewritten as

$$I_L^2(k+1) = I_L^2(k) \left(1 - \frac{2\Delta t}{\tau} (4 - 3D(k)) \right), \quad 7-9$$

where $\tau = \frac{L_{ST}}{R_L}$. The average power $P_{AVE}(k+1)$ at $t(k+1)$, using Eq. 7-5, equals

$$P_{AVE}(k+1) = R_L (4 - 3D(k+1)) I_L^2(k) \left(1 - \frac{2\Delta t}{\tau} (4 - 3D(k)) \right). \quad 7-10$$

$I_L^2(k)$ is substituted, again using Eq. 7-5, to rewrite Eq. 7-10 as

$$P_{AVE}(k+1) = P_{AVE}(k) \frac{4 - 3D(k+1)}{4 - 3D(k)} \left(1 - \frac{2\Delta t}{\tau} (4 - 3D(k)) \right). \quad 7-11$$

In this example, it is in the designer's interest to determine the required duty cycle $D(k)$ from $P_{AVE}(k)$, $P_{AVE}(k-1)$ and $D(k-1)$, where the required discharge power is the goal. Thus Eq. 7-11 is processed to give

$$D(k) = \frac{1}{3} \left(4 - \frac{P_{AVE}(k)}{P_{AVE}(k-1)} \frac{4 - 3D(k-1)}{\left(1 - \frac{2\Delta t}{\tau} (4 - 3D(k-1)) \right)} \right), \quad 7-12$$

where k has been shifted one step back to allow prediction of the current value at time $t(k)$ as a function of that at time $t(k-1)$.

The control method adopted here is to define a desired power transfer curve $P_{AVE}(k)$ and assume an initial duty cycle $D(0)$, calculated from Eq. 7-5 for $I(0)$ the initial discharge current and $P_{AVE}(0)$. From this, Eq. 7-12 is used to generate a look-up table of duty cycles for all the remaining steps. For non-applicable values of $D(k)$ (values less than zero and greater than 1), a limit function must also be incorporated.

This is analogous to the discontinuous area of operation. This is especially important if open loop control is performed, as it is apparent from Eq. 7-12 that if a constant power is required, the duty cycle calculations become independent of the required power. The duty cycle is dependent only on its initial value, which must come in at the correct time.

The transient times discussed in the section 7.2 are used as 'dead time'; no switching can occur within this dead time. It is observed as well that it is not necessary to include the convergence time into this buffer as switching of the states before the currents converge will have no effect on the system's functionality. For the prototype, this translates to a safe dead time of about 3 μ s. It is further observed that this algorithm is applicable to coupled and uncoupled systems as only the total storage inductor value L_{ST} is required for control calculation purposes.

7.4 Algorithm verification

The prototype is configured to a 2-module system. The first switch is Q_1 of the initial configuration. When this switch is switched, it remains off and the control algorithm is initialised. Switch Q_4 is reconfigured to act as Q_{PWM} . The full 32 mH inductor is used, representing a 32 mH in the series discharge state and 8 mH in the parallel discharge state. A load of 1 Ω is used; this has the advantage of allowing for a longer discharge period and keeps the load voltages low. The synchronous open loop control method is used with the goal function P equal to a constant value of 10 kW (this translates to a constant average current of 100 A).

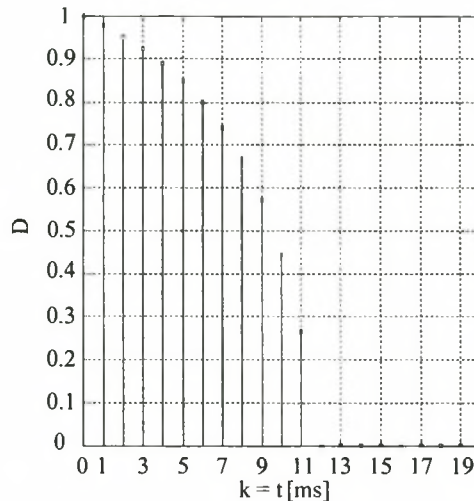


Fig. 7-4 Duty cycle vs time steps

The charge current is chosen as 100 A. The switching frequency is chosen arbitrarily at 1 kHz. The required duty cycle is documented in Fig. 7-4. Each duty cycle is applicable for the duration following it (so the duty cycle at $k = 0$ is applicable to the time duration $0\text{ms} > t > 1\text{ms}$).

It is observed from Fig. 7-4 that for the first interval – for $k = 0$ or at $t = 0\text{ ms}$ – the duty cycle equals 1. This means that the series discharge state is equal to or too large for the required power level. The duty cycle changes continuously until $k = 11$; from $k = 12$ on, the duty cycle is zero which means the parallel discharge state provides just enough or too little current to retain the required power level. Fig. 7-5 shows the measured output voltage level compared to that predicted with using the mathematical model; the result are in good agreement.

It is clear that in the first time segment the duty cycle is 1 (the series discharge state is retained throughout the time step) and that after the 11th cycle (from the 12th millisecond on), the duty cycle is 0; the parallel discharge state remains switched. Thus active shaping of the output pulse is thus only possible for these first 11 ms.

Fig. 7-5 shows the resultant average power during the discharge cycle. Both readings are generated from moving average calculations of the instantaneous power levels. The required power level is 10 kW; good agreement between measured and predicted values is apparent. Although the signal appears noisy, comparison with Fig. 7-6 shows that the actual goal – that of constant energy injection into the load – is well matched.

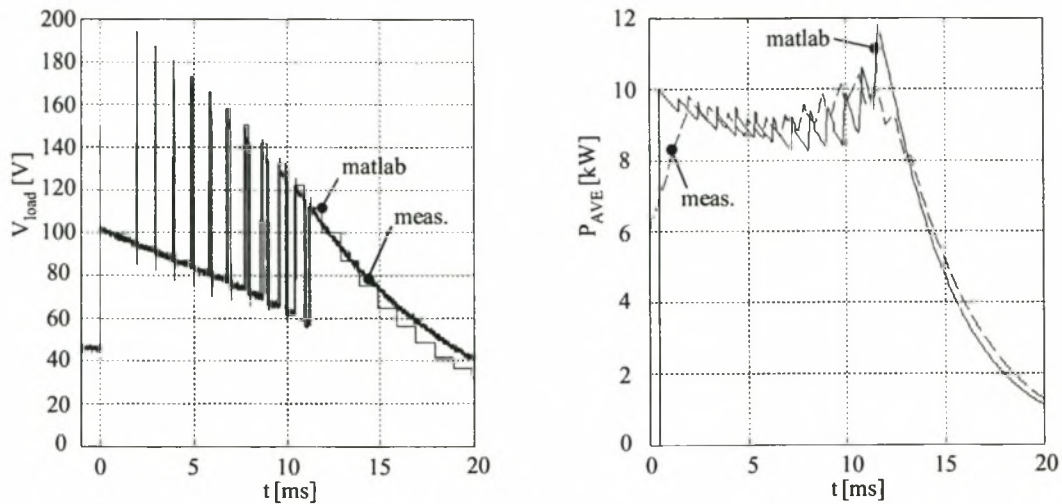


Fig. 7-5 Predicted and measured load voltage and power

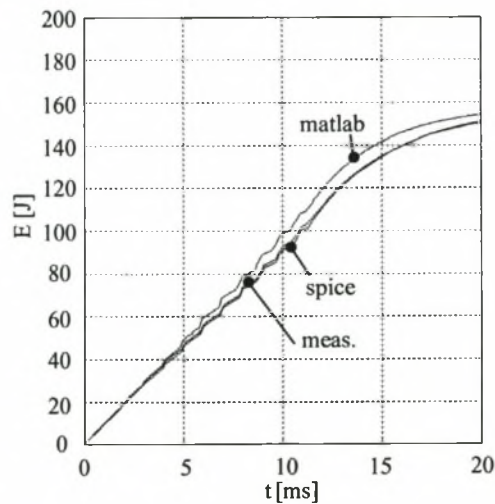


Fig. 7-6 Predicted and measured energy transfer waveforms

The three traces of Fig. 7-6 show the resultant transferred energy wave shapes. The Matlab trace is that discussed represented in the above sections. The spice model uses the required duty cycle values and simulates the system. It is clear that the predicted transferred energy is higher than the measured or spice simulated results; this is most probably due to the approximation of constant level discharge made in section 7.3. Agreement between the predicted and measured values can be improved through increasing the switching frequency or the development of a more accurate model.

It is observed, however, that the measured and spice-simulated values are in very good agreement; the transferred energy follows a linearly increasing path.

7.5 Summary

It is observed through modelling of the relevant transients that it is possible to PWM the output pulse shape as proposed in this chapter; the series discharge, parallel discharge and intermediate transients are all stable and any imbalances that occur die naturally. It has been observed that the diodes must be rated (voltage) equal to the switches.

A preliminary synchronous open loop control protocol is suggested and verified. Further work on an applicable protocol should be performed, however. Fig. 7-6 shows that there is good agreement between predicted and measured values. It is thus proven that PWM of the output pulse to achieve a desirable energy transfer rate is possible. Exact determination of the advantages of PWM of the output waveform over the use of discrete modules is not approached formally. Certain cases can be discussed, however.

If the energy needs to be lumped towards the end of the discharge cycle, for instance, a 4-module system will better achieve this. For pulse shaping during the main discharge length, it is clear through comparison of Fig. 6-10 and Fig. 7-6 that a 2-module PWM'ed system is superior to even a 4-module discrete system. For a balanced system, there is no switch or system volume gain from reducing the module count. However, increasing the module number will in practice result in issues that effectively increase the system volume (not appreciably, however); thus system complexity is reduced (not control complexity) and pulse forming capabilities are increased through the use of PWM.

Implementation of PWM on an actual system will require some scaling considerations. It is observed that active control of the output pulse is 11 ms. A 500 kJ system will require a controlled discharge time of around 5 ms. Thus it seems plausible that for similar results and controllability, the switching frequency should be around 2 kHz. This is a reasonable switching frequency for high-power silicon switches.

CHAPTER 8

CONCLUSION

8.1 Research summary

This thesis conducts a study of volume-optimised inductive storage supplies applicable to ETC loads. The major results are summarised in the following list:

1. A modified XRAM topology original to this thesis which requires less volume than its standard counterpart is presented and analysed. Circuit functionality and component stability are analysed and it is proven that the circuit is a viable option, with the requirement that the load itself incorporates some voltage protection.
2. As volume concerns are a prime system criterion, a volume model and a number of variations are presented.
3. A low-energy prototype is constructed and the electrical analyses and volume model are validated.
4. A hypothetical full-ratings system using contemporary technology is presented.
5. Lastly, a novel PWM pulse forming technique that allows for better pulse shaping with no increase in system module number is presented and validated.

A more in depth summary of each chapter is now presented.

Chapter 2 performs a background study on the broad issues around electric gun systems and isolates system criteria applicable to this project. International projects of the last decade are presented, with the aim of researching the most applicable topologies, sub-system technologies and performance envelopes. Research conducted under Soreq from 1989 to 1997, documented in international journals and publications, is chosen as the model to base this research on.

Chapter 3 presents the standard XRAM and modified XRAM topologies and describes the topological and functional differences between the two. The relevant switching and discharge states are analysed and possible problems identified. It is shown that all the states are sufficiently stable and that the effects of parasitics and possible device value inaccuracy are predictable and controllable. Specific concerns including thermal stability of the switches, voltage-sharing issues, control and

instrumentation issues and fault situation handling are analysed and limit envelopes are generated.

Chapter 4 presents the existing volume model developed by the Soreq team. Slight improvements are made on this model to make it more general and an alternative model is developed that incorporates parameters not possible with the Soreq or continuous model. Specifically, it is shown that the new model can incorporate the effect of Q_{V_ON} , which has a non-negligible effect. Additional variations of the model discussed in Chapter 6 can also deal with non-continuous sub-system parameters, a requirement that is shown to be necessary in certain cases.

Chapter 5 draws general results from the above volume models that are applicable to the performance envelopes considered. General results, including the effect of modularity, energy required, battery technology, system charge time and some other applicable parameters on system volume and front-end efficiency are drawn up. Lastly, a 500 kJ system suggestion, including sub-system details incorporating thermal and electrical stability of the circuit, is made. It is shown that using contemporary technologies and semiconductor switches, it is possible to build a system of volume under 1 m^3 .

Chapter 6 discusses the design, construction and testing of a prototype with ratings of 2.5 kV and 1.2 kA. Full ratings were achieved.

Chapter 7 introduces a novel PWM-based pulse forming scheme and validates its applicability to inductive storage supplies through experimentation.

8.2 Scalability concerns

8.2.1 General scaling considerations

The prototype is electrically characterised with ratings of 2 kJ, 2.5 kV, 1.2 kA. A 500 kJ system will be rated at 500 kJ, 20 kV, 40 kA (according to section 5.9). This translates to a ratio of 250:8:33. The energy statistic is, however, misleading; of prime concern are the voltage and current statistics, as the size of the inductive store will further determine energy storage capabilities.

The circuit topology and volume optimisation algorithm are sufficiently validated through the design of the prototype. There is no reason to doubt the validity of this topology or optimisation procedure for any scaled system design, theoretically unlimited in most respects (except, as shown, if the sub-system components are not

sufficiently volume-continuous). This concern is system specific. Each subsystem is now considered independently.

8.2.2 Inductor scaling concerns

For the inductor, isolation, thermal, strength and fringe field considerations are important.

1. Design of the prototype shows that inclusion of isolation can result in excessive volume increase. However, the prototype does not focus on this aspect and it is assumed that sufficient isolation could be incorporated with minimal volume increase.
2. The thermal stability has been shown to not be a serious issue, and only minimal (if any) considerations need to be made.
3. Ref. [10] discusses inductor strength, where it is shown that for volume-optimised systems there is no problem.
4. Coupling between an air-core inductor and its surroundings may present a serious problem. This has not been considered in this research.

8.2.3 IS scaling concerns

Assuming that the IS technology is sufficiently modular, it is assumed that scaling concerns are not an issue. Thermal stability could be an issue, but this is not considered here. Of interest, however, as observed in section 6.7.3, the device internal resistance does alter with energy storage levels, and could alter appreciably. As the optimisation procedure uses this internal resistance as a design parameter, the volume calculations are sensitive to possible variations. It is assumed therefore that the energy content levels are clamped within specific limits and that operation outside of these limits is avoided. This is a coarse approximation and may require further research.

8.2.4 Switch scaling concerns

Switch scaling should be able to continue indefinitely, assuming that voltage and current sharing is well controlled, heat exchange is well defined and that the switches are sufficiently protected against system parasitics. Ref. [52] describes a silicon switch matrix (IGCT technology) that switches up to 50 kA. Refs [66] and [67] describe the construction of a 25 kV MOSFET switch. Thus the groundwork appears laid for a 20 kV, 40 kA switch, although matrix techniques still need to be verified

and volume optimisation, in particular, still requires attention. The switch suggested in section 5.9 does however use contemporary switch packaging with contemporary techniques, and for IGBT devices current sharing is not an issue (although switch synchronisation during turn-off may present challenges). Thus the switch appears a possibility, albeit an expensive option.

However, there are other concerns that are not well defined and do require attention – in particular, the functioning of IGBTs in high magnetic fields. The 500 kJ inductor will generate a field according the approximation

$$B = \frac{L_{ST} I_{REQ}}{N A_L} = \frac{8mH \times 10kA}{120 \times 0.15m^2} = 4.4T, \quad 8-1$$

where A_L is the inner radius area of the inductor. It is shown that it is not required for the switch bank to lie adjacent to the storage element, so the switch bank could lie well removed from the inductor, assuming that the connection leads form part of the storage inductor itself.

8.3 Thesis contribution

The work presented in this document is largely based on research conducted by Kanter *et al*, where the XRAM topology is initially suggested and a single model volume optimisation is performed. Kanter *et al*. Also document the construction of a 500 kJ system and test results have been published.

This thesis contributes to this field in the following ways:

1. A modified version of the XRAM topology that requires fewer active switches than its counterpart is presented and its functionality is verified.
2. The volume model developed in [10] is expanded to incorporate the effect of an unmatched front-end.
3. An alternative volume capable of incorporating the effect of Q_{V_ON} and non-continuous sub-system volume parameters is developed and verified.
4. It is proven that a balanced system is required for a volume optimum if the system is modular. Similarly, it is proven that for a matched system, system volume is independent of module number.
5. The use of IGBTs – and the related implications – as the active turn-off switch is researched.
6. It is shown that PWM of the load pulse is possible and allows effective pulse shaping utilising fewer system modules.

8.4 Future work and re commendations

8.4.1 Battery IS, inductive s storage PFN

The level of technology concerning the IS and the inductor itself is sufficiently advanced to allow for the construction of the specified systems.

In particular, however, the effect of the inductors fringe fields on, firstly, the system in general and, secondly, the switches is not well researched and requires work.

Coupling of this field to a vehicle chassis or spatially adjacent hardware is unmodelled and requires attention. It is unlikely that the field will result in EMI-related effects (as regards radiation), but the presence of a strong magnetic field in any system requires attention. Semiconductor switches involve complex current flow paths that may be influenced by these fields; topic-specific research needs to be conducted here, although a viable alternative is to physically move the switch bank from inductive source.

Alternatively, a different inductor geometry could be used, as described in Table 3-1. The effect that this has on the volume module is surprisingly small (although it has an appreciable effect on the actual volume). Switch orientated research could include the following:

1. Development of an accurate thermal model of the switch.
2. Research the effect of high DC H-fields on a turn-off switch.
3. Research the possibility of high volume efficiency switch integration.
4. Validate multilevel switch serialisation.

Alternatively, analysis of ETC waveforms shows that the voltage high occurs mainly during the ETC initialisation stage, when the fuse is busy evaporating. From then on, the system exhibits a comparatively low voltage of less than 10 kV. As a result, the on switches are generally over-rated to match this initial voltage high. If the load initialisation could be performed using a separate supply – a low-energy capacitive storage supply, for instance – and the rest of the pulse form through an inductive supply, a lower overall system volume may be achievable.

8.4.2 <1 MJ PFNs

Capacitive storage PFNs are superior in most ways to inductive storage supplies except, most importantly, for the fact that they have a comparatively low energy

density. Inductive storage appears to solve this problem initially but it becomes clear that the additional switch requirements are excessive. Ref. [49] documents the construction of a capacitive storage device capable of reaching a 1.2 MJ.m^{-3} density including switch gear and shielded inductor. It appears therefore that if capacitor-based systems are a viable technology, they should be considered above equivalent inductive storage systems.

APPENDICES

APPENDIX A

First switch cycle inductor balancing

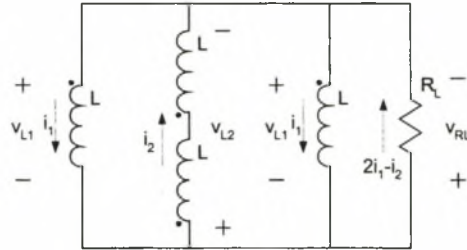


Fig. A-1 Inductor balancing circuit equivalent

Fig. 3-13 a[ii] shows the circuit used to model the inductor-balancing phenomenon. At the time of switching of Q_1 , there is current flowing through the load and – even with balanced inductors and series diode protection for the switches – different currents through certain branches of the storage inductor where $i_1 > i_2$. It is required for this current difference to reduce to zero so that the steady state model as described in Fig. 3-13 (a[i]) becomes applicable.

Reference to section 3.7 shows that the two time constants of concern – that involving the ESRs and that involving the load – are at least an order apart. The inductor ESRs have been ignored as the only current change that can occur – and as a result the only energy transfer between the inductors and thus inductor balancing – requires resistive losses to result in the required voltage drops. These resistive losses are dominated by R_L .

It is required to determine how long the imbalance remains, if the imbalance actually does reduce to zero and what the predominant factors that influence this imbalance are. It can be intuitively observed from Fig. 3-13 a[ii] that once $i_1 = i_2$ the imbalance is over, the diodes D_{B1} and D_{T4} become reverse biased and the circuit equivalent becomes that represented in Fig. A-1. The describing equation of the time of balance correction, or t_{L-L} , can provide all the information that is required. Fig. A-1 indicates that the branch currents of the first and third branch are the same; this is assumed from the symmetry that exists in the circuit.

From Fig. A-1 the describing equations

$$v_{L1} = L \frac{di_1}{dt} + M \frac{di_1}{dt} + M \frac{di_2}{dt} + M \frac{di_2}{dt} = (L + M) \frac{di_1}{dt} + 2M \frac{di_2}{dt}, \quad \text{A-1}$$

$$v_{L2} = 2L \frac{di_2}{dt} + 2M \frac{di_2}{dt} + 2M \frac{di_1}{dt} + 2M \frac{di_1}{dt} = 2(L + M) \frac{di_2}{dt} + 4M \frac{di_1}{dt}, \quad \text{A-2}$$

and

$$v_{R_L} = R_L \cdot (2i_1 - i_2), \quad \text{A-3}$$

can be derived where

$$v_{L1} = -v_{R_L}, \quad \text{A-4}$$

$$v_{L2} = v_{R_L}, \quad \text{A-5}$$

and the initial conditions $I_{L1}(0)$ and $I_{L2}(0)$ complete the description. Two variable relations are included in the results consideration. The relations

$$M = k_c L, \quad \text{A-6}$$

from chapter 3 and now

$$I_{REF} = \frac{I_{L1}(0)}{I_{L2}(0)}, \quad \text{A-7}$$

are incorporated. $I_{REF} \geq 1$ and can only be positive, and $0 \leq k < 1$. This parameter is used as it allows for full cancellation of actual current magnitudes from the following analyses. Maple is used to process the equations. Firstly, Eqs A-1 to A-5 are transformed to the Laplace domain and two describing equations formed. Maple is used to generate the solutions of $i_1(t)$ and $i_2(t)$. The equation $i_1(t) = i_2(t)$ is processed to calculate the time of inductor balance

$$t_{L-L} = 2 \frac{L}{R_L} \frac{(-1 - 2k + 3k^2)}{(5 + 13k)} \left(-\ln(3) + \ln \left(\frac{5I_{REF}k + I_{REF} + 4k + 2}{(3k + 1)(2I_{REF} - 1)} \right) \right) \quad \text{A-8}$$

Fig. A-2 is calculated assuming $k_c = 0.85$ (for the left hand side graph) and $I_{REF} = 325/300$ for the right hand side graph. The two dependencies are clearly illustrated. Fig. A-3 shows measured and calculated results system values of $R_L = 2.6$ (from correlation with section 6.7.4), $L = 2$ mH, $k_c = 0.96$ and $I_{ref} = 52 / 30$. The two graphs are in good agreement. The rounding evident in the measured result is as a result of the snubber capacitors; Spice simulations exhibited similar tendencies.

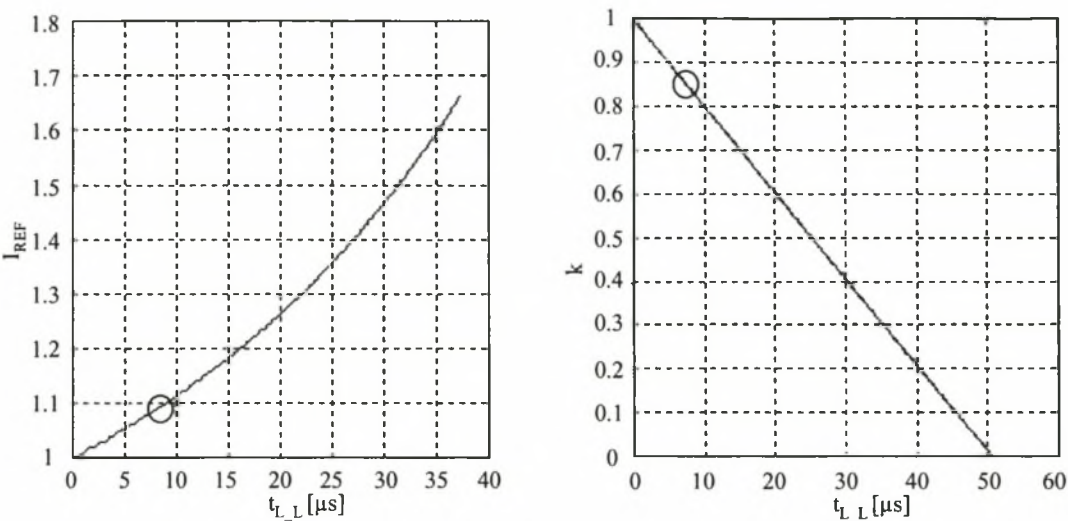


Fig. A-2 Inductor balance time dependencies

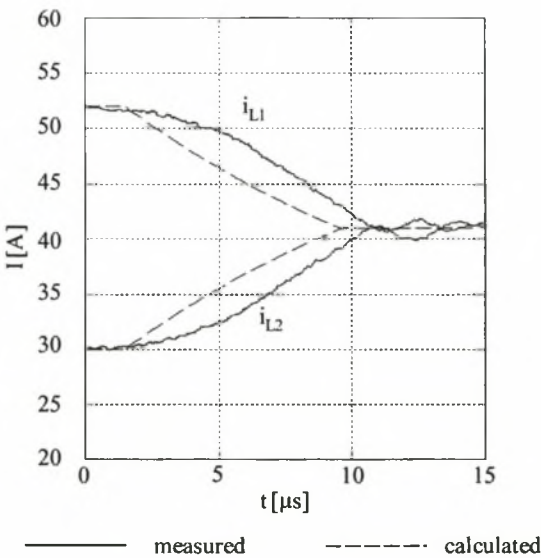


Fig. A-3 First switch cycle measured inductor balance

APPENDIX B

Small inductor value imbalance considerations

In the actual system, inductor modules may not be perfectly balanced. This may result in a current imbalance in the discharge state that results in undesirable – and uncontrolled – discharge patterns. To research the effect of even a slight imbalance in the value of L_A and L_B , Eqs 3-27 to 3-30 are solved (with the assumption that $R_{ESR} = 0$) assuming that $L_A \neq L_B$.

It can be intuitively understood that the rate at which the inductor currents reduce is dependent on both the coupling between the branches and the difference in inductor value. The number of variables makes the derivation of general results difficult. The path considered here is that a certain current difference in the two branches occurs. This is represented as a ratio defined as

$$I_\delta = \frac{i_A(t) - i_B(t)}{I_0}, \quad \text{B-1}$$

where I_0 is the value of both $i_A(t)$ and $i_B(t)$ at the beginning of the switch cycle. The result is

$$I_\delta = 2 \frac{(L_A - L_B) \left(1 - e^{-\frac{R_L(L_A + L_B - 2M)}{L_A L_B - M^2} t} \right)}{L_A + L_B - 2M}, \quad \text{B-2}$$

which is monotonically decreasing and will achieve a steady state as $t \rightarrow \infty$. This steady state can be intuitively described if no current flows through the load and a constant current flows through the inductors. However, this will not occur in the actual system due to the diodes; when an inductor attempts to reverse its current direction the diode will block the current and the system equations will change. It is not in the designer's interest to operate in this area and it is not considered further.

The tool that can be of interest to the designer is the time at which this branch current difference (represented by I_δ) occurs (it is known the current difference only grows from this time on). Eq. B-2 is processed to generate the general solution

$$t_\delta = \ln \left(1 + \frac{1}{2} \frac{I_\delta (L_A + L_B - 2M)}{L_A - L_B} \right) \cdot \frac{L_A L_B - M^2}{R(L_A + L_B - 2M)}, \quad \text{B-3}$$

which can be a non-real number if I_δ is of a value not achievable with certain system value combinations.

Thus for a known system the designer can decide what the maximum allowable current difference is and further determine the maximum delay before the next module is switched. Further analysis of Eq. B-3 is possible. The substitution of $M = k_c \sqrt{L_A L_B}$ and of $L_B = u L_A$ where u is inductor value ratio into Eq. B-3 results in the solution

$$t_\delta = \frac{L_A}{R} \left(\ln(2) - \ln \left(\frac{I_\delta (1 + u - 2k_c \sqrt{u}) + 2(u - 1)}{u - 1} \right) \right) \cdot \frac{u(k_c^2 - 1)}{(2k_c \sqrt{u} - u - 1)}. \quad \text{B-4}$$

Eq B-4 can also result in a non-real number, however; these solutions are not valid.

Fig. B-1 displays the dependency of t_δ on the coupling factor k_c and the inductor imbalance ratio u . Typical system values (as per section 5.9) of $L_A = 2$ mH and $R_L = 0.1 \Omega$ are used. The allowed current imbalance for both graphs is set at 0.1, or 10%. For the k_c graph, $u = 0.9$ (considered typical) and for the u graph, $k_c = 0.85$ (also typical). These points are cross-referenced on each graph with a circular marker. As the coupling increases, the current imbalance occurs faster, which is an undesirable situation. At $k_c = 1$, $t_\delta = 0$ which means that the current imbalance occurs immediately. It would appear therefore that any difference in inductor value results in a current imbalance that is aggravated by the coupling (in the series-balancing system of Appendix A, the coupling assisted in reducing the current difference; the opposite occurs here).

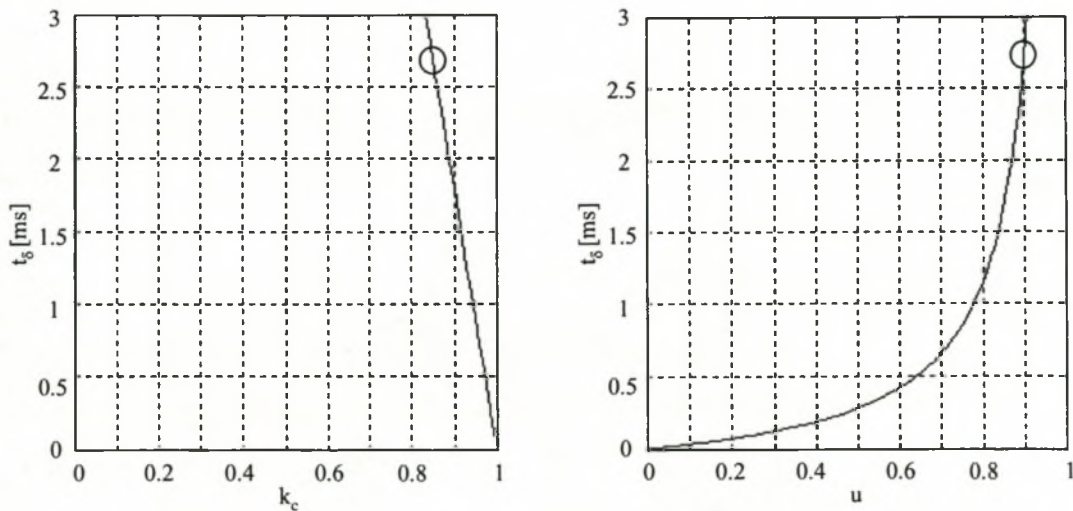


Fig. B-1 k_c and u vs current imbalance time

As the inductor value difference decreases (resulting in an increase in u where a value of 1 relates to perfectly matched inductors and is the ideal), the current imbalance occurs at a later time (which is desirable). Both of these results can be intuitively derived. For a typical 500 kJ system, it is observed that for an allowable current imbalance of 10%, a coupling factor of 0.85 and inductor imbalance factor of 0.9, the next stage – switch stage 3 – must occur within 2.7 ms.

APPENDIX C

Voltage overshoot considerations

For known parameters it is possible to determine if the over-shoot transient takes place while the switch itself is busy switching. To circumvent this pre-requirement of a known system it is assumed that switch has completed commutation and that the current source $i_{L_s} - i_{Q_1}$ is a step input function; this is the worst case. The full passive system z_p is modelled as a Laplace-plane load equal to

$$Z_p(s) = \frac{R_L + sL_L}{L_L C_{SNUB} s^2 + R_L C_{SNUB} s + 1}, \quad \text{C-1}$$

and the load as a unit step input with magnitude equal to the inductor currents magnitude

$$I_p(s) = \frac{I_{SRC}}{s}, \quad \text{C-2}$$

assuming $i_p = i_{L_s} - i_{Q_1}$ where $i_{L_s} = I_{SRC}$ and $i_{Q_1}(t) = (1 - u(t)) \cdot I_{SRC}$. The initial conditions are ignored. The resultant voltage is given as

$$V_{C_SNUB}(s) = \frac{I_{SRC}}{s} \frac{R_L + sL_L}{L_L C_{SNUB} s^2 + R_L C_{SNUB} s + 1}, \quad \text{C-3}$$

where $V_{C_SNUB}(s)$ represents the voltage across the snubber capacitor and thus also Q_1 . It is this voltage that we wish to consider.

Although the system appears simple, calculation of an analytical solution to determine the required capacitance for a known system and defined overshoot is difficult. Using standard second order system approximations [78] such as rise time, settling time and overshoot approximations is not possible as the system has a zero which, for typical parameter values, is not negligible. Direct calculation of the system overshoot is possible. Maple is again used. Firstly, Eq. C-3 is inverse transformed back to the time domain. This results in the general solution of

$$v_C(t) = R_L I_{SRC} + I_{SRC} e^{-\frac{t}{\tau}} \left(L_L \omega \sin(\omega t) \left[\frac{4L_L - 2C_{SNUB} R_L^2}{4L_L - C_{SNUB} R_L^2} \right] - R_L \cos(\omega t) \right), \quad \text{C-4}$$

where

$$\tau = \frac{2L_L}{R_L}$$

$$\omega = \frac{1}{2} \sqrt{\frac{4L_L - R_L^2 C_{SNUB}}{L_L^2 C_{SNUB}}} \quad \text{C-5}$$

Processing of this equation is possible. Taking the derivative of Eq. C-4 and equating the result to zero and making the time t the subject of the formula gives the times where peaks and troughs occur. This time is recurring. The result of

$$t_{PEAK} = 2 \frac{n\pi + \arctan\left(\frac{R_L^2 C_{SNUB} - 4L_L}{R_L L_L \omega}\right)}{\omega}, \quad \text{C-6}$$

where n is a positive integer can be substituted into Eq. C-4 to determine the magnitude of the relevant peaks and troughs. At $n=1$ the first – and intuitively the highest – peak will occur. It would be in this projects interest to obtain an analytical solution of the required capacitance C_{SNUB} for a defined overshoot, L_{L_S} and R_L ; however, manipulation of the above equations is impractical. Likewise, a closed form solution to the rise and settling time of this transient is also impractical to achieve.

As a very rough and worst case approximation, reducing R_L to zero gives the voltage response description as

$$v_C = I_{SRC} \sqrt{\frac{L_L}{C_{SNUB}}} \sin\left(\frac{1}{\sqrt{L_L C_{SNUB}}} t\right). \quad \text{C-7}$$

Which is a sinusoid of magnitude $I_{SRC} \sqrt{\frac{L_L}{C_{SNUB}}}$. As a result, it can intuitively observed that the overshoot – with no damping of the oscillations – will be (worst case) the superposition of the steady state solution plus the sinusoid magnitude which is equal to

$$V_{C_PEAK} = I_{SRC} R_L + I_{SRC} \sqrt{\frac{L_L}{C_{SNUB}}}. \quad \text{C-8}$$

This can be manipulated to determine the required capacitance for the desired voltage overshoot level of V_{C_PEAK} . The actual overshoot – due to the damping – will always be less than V_{C_PEAK} . This approximation may appear extreme. However, for the first switch cycle transients, the voltage overshoot is not of immediate concern. In the prototype, a snubber capacitor is required across the switches for sharing purposes

anyway. If the resultant sharing capacitor is of a greater value than the C_{SNUB} required for worst-case voltage overshoot calculated using Eq. C-8, it is certain that there will be sufficient over-voltage compensation.

APPENDIX D

Device thermal calculations

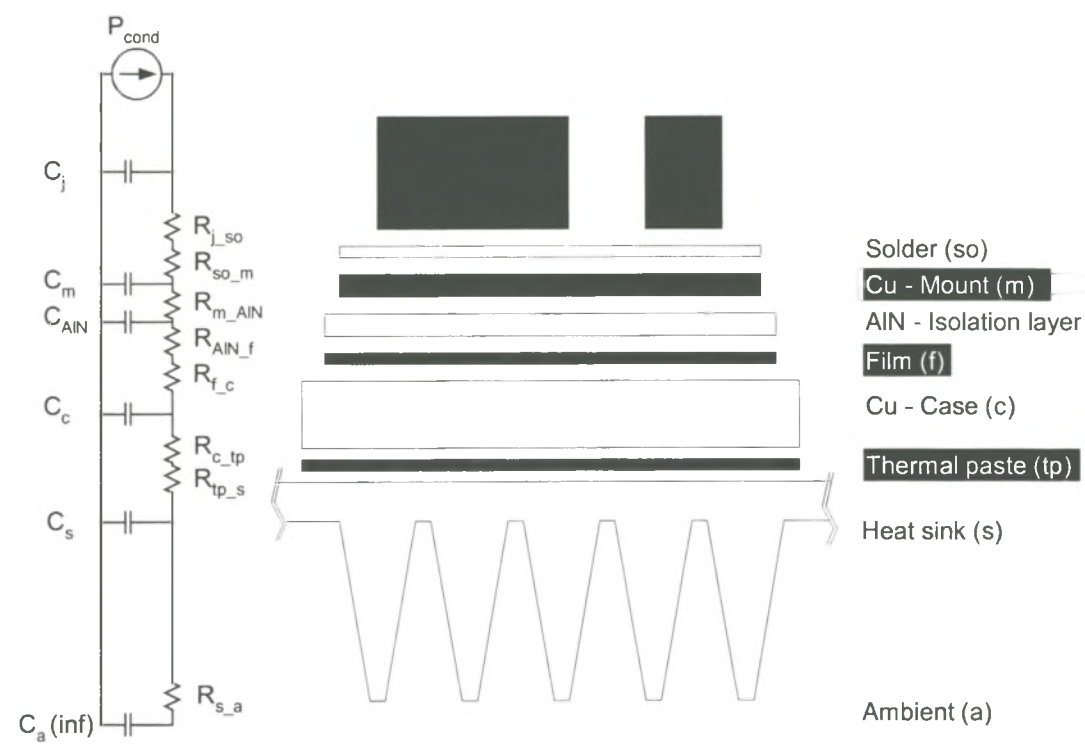


Fig. D-1 Thermal flow paths

Described in Fig. D-1 is the full energy flow path from the origin of the power dissipation in the silicon (P_{cond}) through the respective layers and eventually into the air, or the ambient temperature. It is a combination of an IGBT model discussed in [61] and the heat transport model discussed in [74].

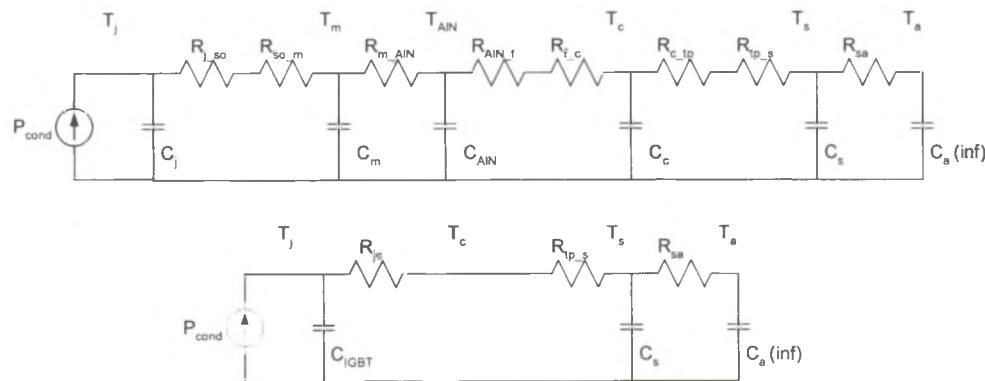


Fig. D-2 Thermal models

The temperatures of each layer have been indicated in Fig. D-2 and they are analogous to voltages before the thermal resistance approximations. The air, or the ambient level, is equivalent to a capacitance of infinite value. It is seen that Fig. D-2 resembles a low-pass filter. Effectively, the designer wishes to utilise the device heat capacities to ‘filter out’ short pulses of high power excitation. Exact quantified representations of each term is dependent on a number of factors including the material properties, material surface conditions and the layers geometric quantities; it is understandably difficult. In general, an approximation of the order of

$$R_{jc} = R_{j_so} + R_{so_Cu} + R_{Cu_AlN} + R_{AlN_f} + R_{f_c}, \quad \text{D-1}$$

is made (as indicated in Fig. D-2). This can be empirically determined. Furthermore, the individual device capacitances are lumped into a single device C_{IGBT} .

It is clear however that a single stage device model of a resistance and capacitance is very limited and does not describe the actual heat transport process accurately.

Device datasheets instead document a thermal impedance which is not composed of a real and imaginary component analogous to this capacitance and resistance but is actually an empirical measurement of a step power input response (generally normalised to R_θ). Fig. D-2 is processed to develop a first order (a single capacitor and resistor) model of the 1.2 kV device with $R_\theta = 0.078$. Here R_{sa} is taken as zero and the sink and ambient capacitors as infinite. Z_θ is read from the datasheet and plotted on a linear scale using Matlab. The original data is itself course so the results can only be taken as indicative.

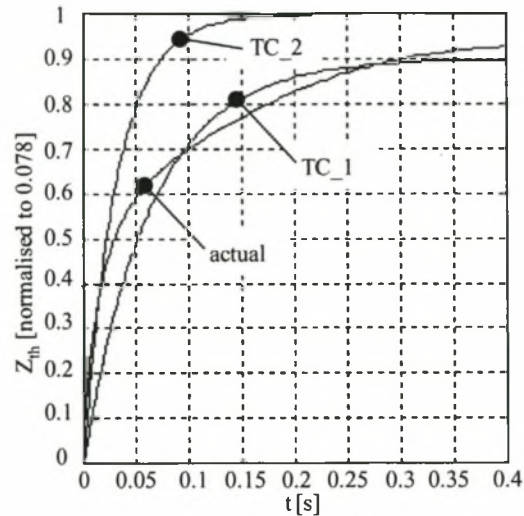


Fig. D-3 Temperature transients (normalised to R_{θ})

Shown in Fig. D-3 are three responses. It is clear that the actual transient is composed of at least two time-constants – the first transient is quick (modelled using TC_2 with a time constant of 30 ms) and the second a slower transient (roughly modelled using TC_1 with a time constant of 60 ms and magnitude modifier of 0.9). Although it is clear that the single capacitor model is not totally adequate, it is clear that the thermal response reaches near-steady state at latest 200 ms. Thus it becomes clear that any power-excitation that is of this order or larger must consider the device as in its thermal steady state. As a result no advantage can be gained from the material heat capacities within the device. However, if a high current switch is to be constructed, a more intensive study to exactly determine the switch unit performance envelope should be performed. Ref. [61] documents a method.

APPENDIX E

Opening switch voltage sharing issues : Sharing Methods

Passive outside

By 'outside' is meant by control of the power terminals to the device (as opposed to the gate or controller terminals). This sharing method is applicable to all devices and can be further separated into diode or capacitor clamped converter systems (documented in [79]) or snubber-based dv/dt limiters. An inductive storage PFN topology does not require a bus and thus converter-based solutions are not applicable.

However, dv/dt limiters are recognised as the most robust sharing methods and are preferred for very high voltage applications [66]. They take the form of resistor-capacitor-diode (RCD) snubbers, in various applicable topologies. Ref. [79] documents various capacitor charging schemes and suggests a novel self-clamped RCD snubber that proved effective.

Of distinct importance here is the difference between the XRAM topology researched here and conventional converter requirements. Firstly, the switches only switch once. Secondly, the device hold-off voltage is equal and parallel to the load voltage and this voltage falls to zero at the end of the discharge cycle. As a result, the capacitor of the RCD snubber need not be discharged (its voltage falls with the load voltage and its stored energy is effectively transferred to the load) and the R and D parts fall away. Thus simple capacitor snubbers are all that is required for the XRAM topology. This method is implemented in the prototype and proved successful.

However, for power levels required by the final system, the capacitor volume required for similar sharing reliability will prove excessive. Some alternative methods are thus proposed and discussed. An alternative is the use of a MOV or other lossy voltage-clamping device. However, the reliability of even high power MOVs in this application is low and the option is not considered further.

Device matching

This method is described sufficiently in Ref. [79] and not considered further here. Of worthwhile mention however is a novel method of voltage sharing proposed in Ref. [67] which documents the construction (and successful application) of a 25 kV 138 A

switch using serialised MOSFETs. The focus of this research is mainly on the synchronisation of the gating signals. The method used here is displayed in Fig. E-1.

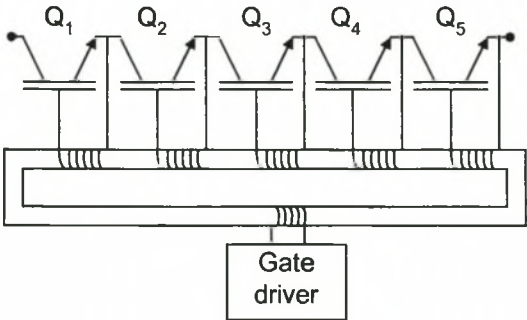


Fig. E-1 Synchronised device gating

Effectively, the gate signals are all synchronised through the use of a common magnetic core on all the drivers. No problems or difficulties one would expect – such as leakage inductance, reaction time or the capacitive load – were documented and a switching time of 50 ns was recorded.

The system was taken up to 2 kHz with no device failure. The advantages of such a system are also clear; the level of modularization is not limited and no feedback is required. The disadvantages are that the devices will obviously have to be well matched and the magnetic design will have to be very precise to minimise the effect of the magnetic parasitics. Also, no record of this methods application to IGBTs or HVIGBTs has been found.

Passive gate driving schemes

This option can be separated into two classes. The first concerns the passive feedback of a device to itself.

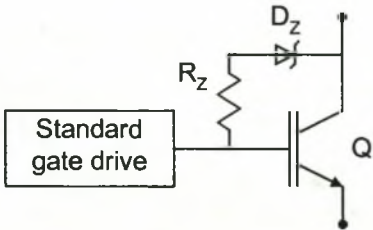


Fig. E-2 Passive feedback control

The proposed circuit of Fig. E-2 is comprised of a simple over-voltage feedback path that senses an over-voltage and passively injects current into the device gate, effectively switching the device back on to again reduce the device V_{CE} . The

device D_z is a zener-based device ('Transils' are commercially available that are specifically made for this application).

Ref. [66] mentions this option and quotes a 25 kV 1200 A application using MOSFETs that utilises this sharing method. This method obviously requires detailed knowledge of the specific device to be serialised to prevent possible instabilities. The advantages of such a system are clear; the level of modularization is not limited, very little extra hardware is required and no high-voltage feedback is required (as information). The disadvantages are that the series stack will switch as fast as the slowest switch only resulting in increased system losses and reduced device lifetime. Also, no record of this methods application to IGBTs or HVIGBTs has been found.

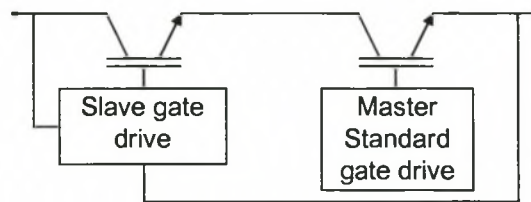


Fig. E-3 Bootstrap methodology

The second method for passive gate control is the bootstrap method described in both [79] and [66] and shown in Fig. E-3. This requires high voltage feedback and effectively allows the passive control (through a resistor network or similar) of a slave device to be linked to a master device, which is switched with a standard gate driver.

The master device is switched slower than the maximum switch time of the slowest device to ensure that the slave device does switch. This circuit topology's advantage is in its simplicity and passive feedback. Increasing the device number is theoretically possible but requires more complex electrical connections. The disadvantages of this system are that the switching losses are increased and switch robustness may become an issue.

Active gate driving schemes

Again there are two classes for active gate switching. The first is documented in [66] and is similar to the bootstrap topology shown in Fig. E-3, but uses active gate control on the slave device. This allows for improved control of the slave device and faster switching. However, intelligent voltage feedback is required and similar problems with increasing the module number result. This method can also be expanded to allow for a master-master approach that processes both device voltages to develop the gate

voltages. The disadvantage of this method is the gate-signal dependence on the high voltage feedback.

The second active gate control method is documented in [66] and specific examples (and slightly different methods) are proposed in [68]-[71]. The difference in the respective methods is basically the method in which the gate signal is formed. Refs [70],[71] and [57] uses op-amps (with the usual band-width limitations) and connected circuitry to generate a voltage reference and Refs [68] and [69] use discrete components.

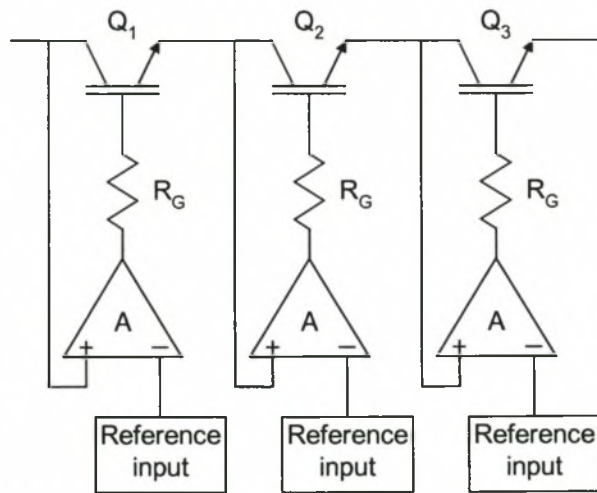


Fig. E-4 Individual cell active gate control

Fig. E-4 shows the control strategy for the control of each unit. The reference input is necessarily made slower than the slowest device switching behaviour. The reference input is designed to match the devices expected voltage rise performance. The multiplier block A is a sensitivity block and could incorporate some control algorithms for noise filtering or stability concerns. The advantage of this method are quite clear; the device serialisation number is not limited (theoretically), the device switch transient can be stabilised effectively and only local voltage feedback is required (there is no inter-device dependency). The disadvantages are also obvious, however; the device needs to be accurately characterised beforehand, the switching losses are understandably high and the intelligent voltage feedback means the feedback system is sensitive to EMI.

APPENDIX F

Possible inductor imbalance considerations during turn-on

It is invariable that some current difference (where $i_{L1} - i_{L2} \neq 0$) does occur during the parallel discharge state; this will result from even a small inductor mismatch as described in Appendix B. For the state Fig. 7-1(d) to exist, this current difference must reduce to zero. This occurrence is analogous to that discussed in Appendix A where the current difference converges. During this convergence time, the current difference conducts through one of the diodes into the load. If a current imbalance occurs and assuming that the current imbalance is in the form of $i_{L1} > i_{L2}$, Fig. F-1 represents the discharge paths with D_T reverse biased and D_B conducting.

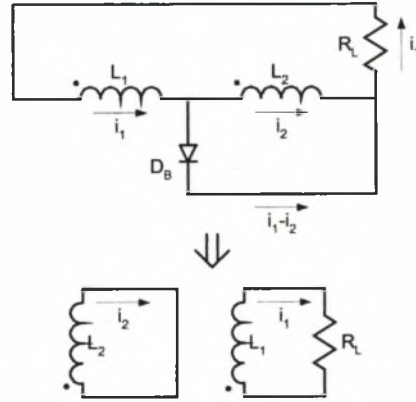


Fig. F-1 Turn-on current imbalance

It is observed that if D_B is conducting, the circuit can be divided into two circuits, coupled only through the mutual inductance M . The two describing equations

$$\begin{aligned} v_{L1} &= L \frac{di_1}{dt} + M \frac{di_2}{dt} = 0 \\ v_{L2} &= L \frac{di_2}{dt} + M \frac{di_1}{dt} = -v_{load} = -R_L i_1 \end{aligned} \quad \text{F-1}$$

are processed to give a solution for $i_{L1} - i_{L2}$ equal to

$$i_{L1} - i_{L2} = i_1(0) \left(1 + \frac{M}{L} \right) e^{-\frac{t}{\tau}} - i_1(0) \frac{M}{L} - i_2(0), \quad \text{F-2}$$

where $\tau = \frac{R}{L - \frac{M^2}{L}}$. If interest to the designer is when the current difference

converges to zero. Defining a current ratio of $I_{REF} = \frac{I_1(0)}{I_2(0)}$ and equating Eq. F-2 to

zero gives the time of convergence as

$$t_{conv} = \frac{L^2 - M^2}{LR_L} \ln \left(\frac{I_{REF}L + M}{L + M} \right). \quad \text{F-3}$$

This current imbalance- as it is expected to be small – will have negligible effect on the transferred energy wave shape. It is of interest in the electrical analysis of the circuit however as it is observed from examination of Fig. 7-2 and Fig. F-1 that if this current imbalance exists, one of the diodes (in this case D_B) will continue to conduct during the whole switch transient. As a result, the other diode - D_T - will hold the full load voltage during switching. Thus the diodes need to be rated at the same voltage as the main switch.

APPENDIX G

Inductance matrix generation

Generation and processing of the characteristic inductance matrix \mathbf{M}_N to form \mathbf{M}_n is discussed in this appendix. This is performed through numerical processing of the inductor geometries, the generated fields and resultant flux linkages to calculate individual mutual inductances between each winding of the inductor to every other winding in the inductor.

A number of assumptions need to be made:

1. Each winding is modelled as planar current loop orthogonal to the z-axis with radius falling in the centre of the conductor it is representing (Fig. G-1).
2. This current loop does not shift in time or space during the charge or discharge cycle.
3. The helical deformation of the actual coil is ignored.
4. The conductors are either circular or square and are modelled as a single current loop.
5. The inductance is defined at the H-field steady-state situation.
6. Full superposition is valid.
7. The conductor material and isolation material is non-magnetic.
8. The inductor has an air-core.
9. Device radial symmetry means that the field need only be calculated in a two dimensional cross-section as shown as the area of interest in Fig. G-1.

Fig. G-1 graphically demonstrates the field distribution of a single conductor (source conductor) in a matrix of a 4×4 square winding area Brooks coil inductor. Of interest is the coupling of the source coil (referred to with a subscript s) to itself (self-inductance) and to the target coil (mutual inductance) (referred to with a subscript t).

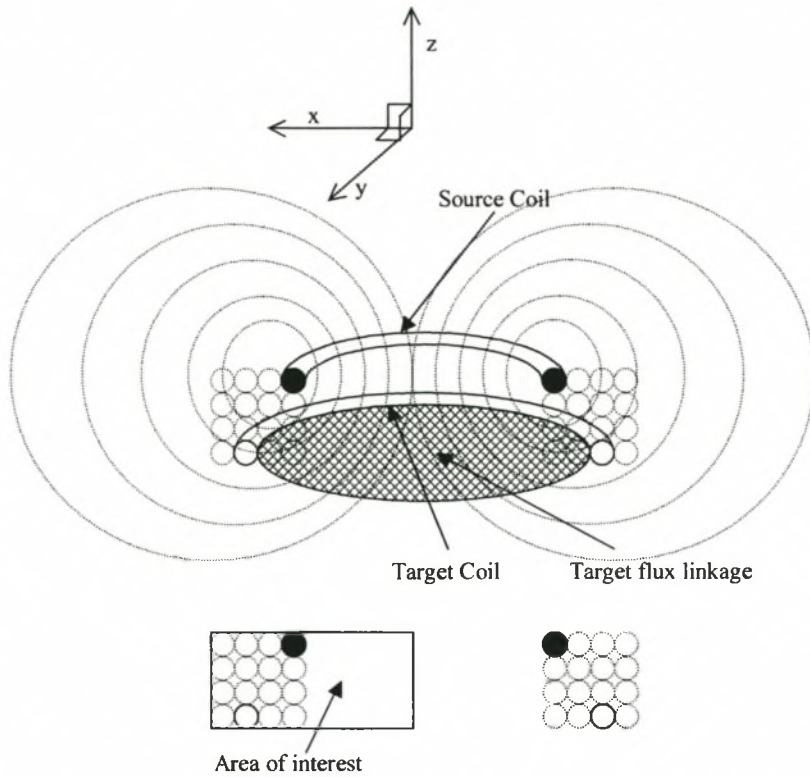


Fig. G-1 Field distribution between two conductor loops

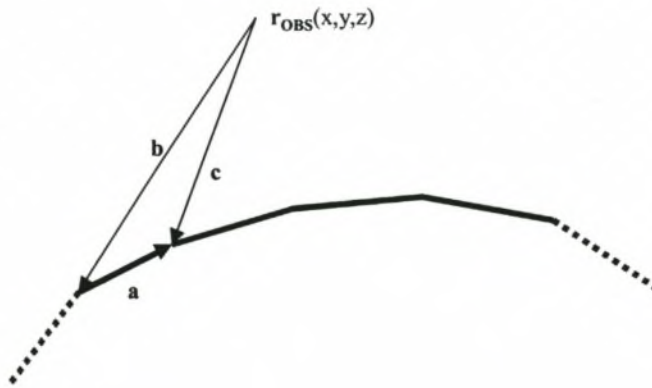


Fig. G-2 Current stick model definitions

The source coil is approximated as a number of current sticks; a value of 40 was proven to be sufficient. Using

$$\mathbf{H} = \frac{1}{4\pi} \frac{\mathbf{c} \times \mathbf{a}}{|\mathbf{c} \times \mathbf{a}|^2} \left(\frac{\mathbf{a} \cdot \mathbf{c}}{|\mathbf{c}|} - \frac{\mathbf{a} \cdot \mathbf{b}}{|\mathbf{b}|} \right) \quad \text{G-1}$$

from [75] pg. 322 with reference to Fig. G-2 it is possible calculate to the value of \mathbf{H} (normalised to 1 A) generated by the source loop for the whole area of interest.

The flux linkage (using the normalised \mathbf{H} [75] pg. 333) of a field to a target is defined as

$$\lambda = \int \mu_0 \mathbf{H} \cdot d\mathbf{a}, \quad \text{G-2}$$

where μ_0 is the permeability of free space and the surface area of interest is that enclosed by the target conductor (shown Fig. G-1 as the planar Target flux linkage). The area differential $d\mathbf{a}$ is orthogonal to this plane; in Fig. G-1 this relates to the z direction. As a result it is only the z -component of \mathbf{H} (H_z) that needs to be calculated; this simplifies the calculation process.

It is thus possible to calculate the flux linkage of any source coil to any target coil, including itself. Assuming that the flux linkage is normalised to 1 A the inductance L is numerically equal to the flux linkage λ . This can be written as a numerical relation of the form of

$$M_{s,t} = \mu_0 \cdot \sum_{n=0}^P H_{z_s}(n) \cdot \pi \cdot (r(n)^2 - r(n-1)^2), \quad \text{G-3}$$

where P is the number of points the target coil radius is divided into, $H_{z_s}(n)$ is the source H -field at the target coil at point n along the target plane, $r(n)$ is the radius at the point n and $M_{s,t}$ is mutual inductance of the source and target coil. It is clear from examination of Eq. G-1 and Fig. G-1 that the mutual inductance of two coils in an air-core inductor is a function only of the spatial relationship between these two coils; it is clear therefore that $M_{s,t} = M_{t,s}$. The mutual inductance of a source coil to itself is called the self-inductance, where $M_{s,s} = L_s$.

To demonstrate the method of matrix decomposition, an inductor consisting of 4 conductors is decomposed to form two coupled inductors of 2 windings each. The voltage across two series inductors (or two coils in an inductor connected in series, as is the case here) is given by

$$v_1 + v_2 = L_1 \frac{di_1}{dt} + M_{12} \frac{di_2}{dt} + L_2 \frac{di_2}{dt} + M_{21} \frac{di_1}{dt}. \quad \text{G-4}$$

With the understanding that in this equation $i_1 = i_2$,

$$v_1 + v_2 = (L_1 + L_2 + 2 \times M) \cdot \frac{di}{dt}, \quad \text{G-5}$$

is used to describe the total apparent self inductance of the two coils. The terms M_{12} and M_{21} are equal and are equated to M . Calculation of the mutual inductance follows

a similar path. To calculate the mutual coupling of the above 2 coils to a third, the equation

$$v_3 = L_3 \frac{di_3}{dt} + M_{13} \frac{di_1}{dt} + M_{12} \frac{di_2}{dt}, \tag{G-6}$$

is decomposed to form

$$v_3 = L_3 \frac{di_3}{dt} + (M_{13} + M_{12}) \frac{di_1}{dt}, \tag{G-7}$$

where again $i_1 = i_2$.

To demonstrate how this is incorporated into the design of \mathbf{M}_n , Table G-1 shows the inductance matrix \mathbf{M}_N of a 4-winding coil.

Table G-1 Characteristic inductance \mathbf{M}_n

Winding # N	1	2	3	4
1	L_1	$M_{2,1}$	M_{31}	M_{41}
2	M_{12}	L_2	M_{32}	M_{42}
3	M_{13}	M_{23}	L_3	M_{43}
4	M_{14}	M_{24}	M_{34}	L_4

Assuming that we aim to develop a 2-module system ($n = 2$) from this 4-winding inductor ($N=4$), we need to couple the windings to form two electrically isolated modules of 2 windings each. To demonstrate, we serially link windings 1 and 2 and windings 3 and 4 according to Eqs G-5 and G-7. This is performed by adding the relevant terms as shown as shaded in Table G-1, \mathbf{M}_N , to form Table G-2, or \mathbf{M}_n .

Table G-2 Characteristic inductance \mathbf{M}_n

Module # n	A	B
A	L_A	M_{AB}
B	M_{BA}	L_B

It is therefore clear that a single inductance matrix of order N contains all the information to describe the coil fully; this matrix is defined as the characteristic inductance matrix \mathbf{M}_N . Calculation of the required \mathbf{M}_n matrix is performed through

the addition of the relevant terms (done physically by the serial connection of the inductor windings); which windings to link are left to the designer of the system.

APPENDIX H

Matlab program listings

H.1 Demonstration Matlab listings for continuous volume model

```
%
% Core code calculating system volume using the continuous model
%
% Written by Julian van der Merwe, 2000
% Project under contract to contractor project number WSR6070
%
% Warning:
% This is the bare code used to generate the volume of a system for
% a defined case. The code is used as the core for the optimisation procedures.
%
% Extended Matlab files are included with the report that calculate
% volume and efficiency comparisons for  $s_{bp}$  and  $E_{stored}$  and  $t_{rat}$ . Running of
% these files will generate the graphs as presented in this report.
% These are
%
% volume_vs_sbp.m
% volume_vs_Eenergy.m
% volume_vs_trat.m
% volume_sorEq.m
%
% This last is a comparison between SorEqs model and the continuous
% model.

% Define system constants required for continuous model

Energy = 500e3;           % Total stored energy
rho = 1.7e-8;             % Resistivities of applicable inductor metals
rhoal = 2.82e-8;
sbp = 80e6;               % Battery power density
k = 1;                    % Front-end ESR ratio ( $R_{MOD}$ )

trat = 1.5;               % Ratio of charge time over system time constant.

lam = 1.5;                % Ratio of Battery volume over inductor volume
%This constant is not actually used; it is inherent in the results.

% Inductor volume modifier = 3.9457e-008 (calculated) or 3.7621e-008
% (Grover) or 6.03e-008 (Soreq). In general the calculated is used.

% Calculate constant
pha = Energy*2*(k+1)^2 / (k*sbp*3.9457e-008/rho*(1-exp(-trat))^2);

% Generate inductor volume sweep and calculate battery volume
```



```
Lvol = 0:0.001:0.5;  
Bvol = pha*Lvol.^(-2/3);  
  
% Calculate Total volume and determine minimum  
Tvol = Lvol+Bvol;  
[a,b] = min(Tvol);
```

H.2 Demonstration Matlab listings discrete volume model

```
%
% Core code calculating system volume using the discrete model.
% It is observed that the code requires specific system detail.
%
% Written by Julian van der Merwe, 2000
% Project under contract to contractor project number WSR6070
%
% Warning:
% This is the bare code used to generate the volume of a system for
% a defined case. The code is used as the core for the optimisation procedures.
%
% Extended Matlab files are included with the report that calculate
% volume and efficiency comparisons for  $t_{CH}$ ,  $R_{MAG}$  and  $Q_{MAG}$ . Running of
% these files will generate the graphs as presented in this report.
% These are
%
% ESRVOL_discrete_Von_working.m
% ESRVOL_discrete_Von_working_2.m which uses an alternative - yet equivalent
% compensation fro  $Q_{MAG}$ 
% ESRvol_discrete_tcharge.m
%
% And used for the constructed model
% ESRvol_built_discrete_Eff.m
%

% define load parameters
Rload = 0.1; % Peak load resistance
T_dis = 5e-3;

% Define Battery statistics
Power_density = 80000; % in W / l
VolBatt = 1; % battery unit volume
Vbatt = 2; % Battery voltage per unit
ESRbatt = Vbatt^2/Power_density; % Battery ESR
Ibatt = Power_density/Vbatt; % Maximum current battery can deliver

% Define switch statistics
Iswmax = 300; % maximum current switch unit can commutate
VolSw = 8; % switch unit volume
Vswitch = 6; % V drop per switch (in series that is)

% Define System Statistics
N = 4;
k=0.9; % coupling ratio
Energy = 500e3; % Energy requirement for the system
DCEff=0.95; % Back-end efficiency - used to define upper
limit for inductor ESR
TRANS_eff = 1; % Used for back-end transfer efficiency
```

```

effF = 1; % Front-end power matching modifier

% Tuner, modifier
upper_limit = 500; % Maximum Ns

% Physical constants
rho = 1.7e-8; % resistivity of copper in ohm.m
rho = 2.82e-8; % resistivity of aluminium in ohm.m
TempconstCu = 4.92e-15; %Copper temperature rise constant

% Some calculated variables
ESR = N*(1-DCEff)/DCEff*Rload; % Defined ESR for upper-limit mark.
L = T_dis*Rload*N*N/(TRANS_eff)*1e6; % Required storage inductor in µH
Iwant=sqrt(Energy*2/(L*1e-6)); % Calculates required charge current
SVOLF = VolSw*N*ceil(Iwant/Iswmax); % Calculate the exact Switch volume

% Define the function sweep - in this case the discrete series battery connection
Ns = [1:upper_limit];

% Calculate inductor quantities from Grover equations
Resr=ESRbatt*Ns/Np*effF; % Calculate desired inductor ESR
deltaF = ((rho*100)^(5/3)*L./((4.0802e-004*Resr.^(5/3))).^(3/8);
% required conductor diameter
lengthF = pi/rho*Resr.*((deltaF)/2/100).^2;
% calculate length of required conductor
NF = ((L./((0.016994*3/2)*deltaF))).^(2/5);
% calculate total winding count required
radoutF = (NF.^(1/2)).*(deltaF)*2/100; % Outer radius of inductor
ccheckF = (L/1000*deltaF.^4*1e6/25.49).^(1/5)/100;
% Inner radius of inductor (checking)
IVOLF = radoutF.^2*pi.*(sqrt(NF)).*deltaF/100 * 1000;
% Inductor volume in litres
BVolF=VolBatt*Ns*Np; % total battery volume

% Inclusion of Qv,ex simply requires adjustment of the IS voltage
Volt=Vbatt*Ns- N*Vswitch; % calculate IS voltage available for charging

% Calculate Total volume and determine minimum
Tvol = LvolF+BvolF;
[a,b] = min(Tvol);

% Calculates temperature rise in inductor;
CondAreaF = (deltaF/2/100).^2*pi; % conductor area in m2
dTf=TempconstCu*Iwant^2*tFrt./(CondAreaF).^2; % rise in temperature of copper

```

H.3 Matlab listings for PWM duty cycle calculation

```
%
% Code generated for the generation of the duty cycle for
% PWM'ing of an inductive storage PFN
%
% Written 2000-09-16 by Julian van der Merwe
% Project under contract to contractor project number WSR6070
%
% Warnings:
% The continuous and discontinuous modes of operation are possible.
% This program assumes that the system passes from:
% discontinuous to continuous to discontinuous
% If the driving function (power) requires intermittent
% swapping from discontinuous to continuous, this model is not
% applicable.
%
% A Matlab file PWM.m included with the report contains the following
% code plus the code that generates all of the graphs (with measured
% values) in this chapter
%

% Enter system constants

% Storage inductor
L = 32e-3; % Load resistance
R = 1; % Series discharge time constant
tau = L / R; % Number of duty cycles.
Dnum = 100; % Inverse of switching frequency
dt = 100e-3/Dnum; % Initial current at moment of discharge cycle start
Io = 100;

% Define power curve required

% Power curve in this case is a constant power
Pconst = 100^2*R;
k = [1:1:Dnum];
P = Pconst*ones(size(k));

% Initialise duty cycle and currents

% It is assumed that the series discharge state delivers
% more current than is required. This is one of the discontinuous
% states. The duration of this state is calculated and the duty cycle
% equated to 1 for its full duration.
% If this state does not exist, this code still initialises the
% duty cycle correctly.
kstart = ceil(-log(Ip/Io)*tau / dt);
if kstart < 1,
    kstart = 1;
```

```

end;
D = ones(Dnum,1);
if kstart == 1,
    D(1) = (4-P(1)/(R*Io2))/3;
end;

% Required duty cycle calculation loop.

for n = kstart+1:1:Dnum,
% Non-continuous duty cycles are filtered out. This is only
% applicable if the situation described in the Warnings section
% occurs.
    if D(n-1) > 1,
        D(n-1) = 1;
    end;
    if D(n-1) < 0,
        D(n-1) = 0;
    end;
    D(n) = (4 - P(n)*(4-3*D(n-1)) / (P(n-1)*(1-2*dt/tau*(4-3*D(n-1))))) / 3;
    if D(n) < 0,
        D(n) = 0;
    end;
end;
end;

```

H.4 Matlab listings for Inductor matrix calculation

```
%
% Code calculating an inductance matrix for a multi-winding inductor
%
% Written 2000-09-16 by Julian van der Merwe
% Project under contract to contractor project number WSR6070
%
% Warnings:
% The program is resource intensive.
%
% This program is called Hfield. It uses HfieldF.m as its core processor.
% Once Hfield.m has been run, Lshare.m can be used to combine the PCC or JRC loops
% as desired. These programs are included with the report

% Hfield calculates the linkages of all the current loops in a rectangular winding
% window w.r.t. to all the other loops. The linkage to itself is its self inductance.
% This program generates A matrix Mt (Mutual total) of size (Wx*Wy by Wx*Wy) giving
% the full mutual inductance matrix of all the % elements to all the other elements in
% the form:
% Assuming we count vertically in Y and horizontally in X, a specific coil address is
% defined as (Y,X) and its value as [Y,X]; we thus show the coupling between, say coil
% (2,1) and (3,2) is (2,1):(3,2) but written [3,2] in the column of (2,1). Comprendre?
%
% Mt = (1,1): (2,1): (3,1): (1,2): (2,2): (3,2): (1,3): (2,3): (3,3):
%
%      [1,1]  [1,1]  [1,1]  [1,1]  [1,1]  [1,1]  [1,1]  [1,1]  [1,1]
%      [2,1]  [2,1]  [2,1]  [2,1]  [2,1]  [2,1]  [2,1]  [2,1]  [2,1]
%      [3,1]  [3,1]  [3,1]  [3,1]  [3,1]  [3,1]  [3,1]  [3,1]  [3,1]
%      [1,2]  [1,2]  [1,2]  [1,2]  [1,2]  [1,2]  [1,2]  [1,2]  [1,2]
%      [2,2]  [2,2]  [2,2]  [2,2]  [2,2]  [2,2]  [2,2]  [2,2]  [2,2]
%      |      |      |      |      |      |      |      |      |
%      [3,3]  [3,3]  [3,3]  [3,3]  [3,3]  [3,3]  [3,3]  [3,3]  [3,3]
%
% You may notice some repetition occurs. We see row one is numerically equal to column
% 1, row 2 to column 2 and so forth as the coupling between two loops is the same
% calculated from either side. Due to the numerical approach used here these will not
% be exactly equal; the error can be reduced by increasing Xmax or increasing the
% number of sticks used in the calculation of Hz for all space in HfieldF.m (increase
% n).
%
% Also calculated is a matrix LMJRC or LMPCC. LMJRC assumes that the inductor is
% separated into electrically isolated units in vertical JRC-type coils (Jelly roll
% oil - that is, wound vertically) to produce Wx separate coils. The matrix LM is a Wx
% by Wx matrix with the self inductance of each of these coils and its mutual
% inductance with the other coils. It takes the form (again for a 3 by 3 inductor)
%
%      (1)      (2)      (3)
% LMJRC = [L1]   [M21]   [M31]
%          [M12]   [L2]   [M21]
```

```

%      [M13] [M23] [L3]
%
% where Mxx = Lx
% Notice here that theoretically, M21 = M12. Again the expected errors occur.
% Calculation of LMPCC is similar but just in the PCC plane

% Define inductor dimensions
Wx = 10; % number of windings in the x-plane (PCC)
Wy = 12; % y-plane number (JRC)
Xmax = 200; % total number of points throughout radial area
% to be calculated
pitchx = 0.020; % distance between conductor centers PCC
InnerRad = 0.225+pitchx/2;
OuterRad = 0.5; % outside radius of coil (outer limit of required
% area)
pitchy = 0.02; % distance between vertical (JRC) windings
n = 40; % number of current sticks used in approximation

% Calculates the flux linkage of a single PCC element top all possible PCC and JRC
% elements
for Hori = 1:1:Wx,
    [fluxXY] = HfieldF(Wy,Wx,Hori,pitchy,pitchx,Xmax,InnerRad,OuterRad,n);
    % calculate the Hz - component for each JRC segment

    Step = Hori
    if Hori==1,
        Mt = fluxXY;
    else
        Mt =[Mt,fluxXY];
    end;
end;

% Generates a general Wx-sized JRC-compound inductor matrix
for C = 1:1:Wx,
    for R = 1:1:Wx,
        LMJRC(R,C)=sum(sum(Mt(( (1:Wy)+(R-1)*Wy), ((1:Wy)+(C-1)*Wy))));
    end;
end;

% Generates a general Wy-sized PCC-compound inductor matrix
for Y = 1:1:Wy,
    for Mx = 1:1:Wy,
        Ltemp = 0;
        for C = 1:1:Wx,
            for R = 1:1:Wx,
                Ltemp = Mt( ((R-1)*Wy+Mx), ((C-1)*Wy+Y) ) + Ltemp;
            end;
        end;
        LMPCC(Mx,Y)=Ltemp;
    end;
end;

```

H.5 Matlab listings for H field calculation

```
%
% Code generated for the calculation of the H-field of an air core multi-turn inductor
% for all influential space. Used as a called function for the full inductor generator
%
% Written 2000 by Julian van der Merwe
% Project under contract to contractor project number WSR6070
%

function [fluxXY] = HfieldF(Wy,Wx,WxN,pitchy,pitchx,Xmax,Rad,OuterRad,n)

% HfieldF(Wy,Wx,WxN,pitchy,pitchx,Xmax,Rad,OuterRad,n)
%
% Wx = horizontal winding number
% Wy = vertical winding number
% WxN = current horizontal JRC coil being examined
% pitchy = distance between adjacent conductors in the y plane
% pitchx = same as pitchy but in x direction
% Xmax = number of points you wish to divide the OUTER radius into for calculation
% purposes
% Rad = Inner radius; position of the innermost conductor in the x- direction
% OuterRad = Area over which you need to calculate H
% n = number of current sticks to be used
%
% HfieldF uses the current stick model to approximate a current loop. The number of
% sticks used is equal to n; 8 is generally sufficient but this can be upped to 40 or
% more for accurate approximations.
% Input are the documented variables. The output is the flux linkage of each conductor
% in the JRC coil to each other conductor of the FULL coil; the linkage of all the
% conductors in the JRC coil at position WxN to all the other conductors throughout the
% whole coil. For a 3 by 3 matrix you will get (for WxN =1): remember addressing is
% (Y,X) and value is [Y,X] and coupling is (1,1):(1,2) = (in column (1,1):,
% (1,1):(2,1) = [2,1])
%
%
% FluxXY
%      = (1,1): (2,1): (3,1):
%
%      [1,1] [1,1] [1,1]
%      [2,1] [2,1] [2,1]
%      [3,1] [3,1] [3,1]
%      [1,2] [1,2] [1,2]
%      [2,2] [2,2] [2,2]
%      |      |      |
%      [3,3] [3,3] [3,3]

const; % bring up in
Hz = zeros(Xmax,Wy); % initialise Hfield z-component
L = (2*pi/n); % angle for current stick vertices

% define current stick vertices in x,y,z co-ords
```

```

for N = 1:1:n,
    A(N,:) = [(Rad+(WxN-1)*pitchx)*cos(N*L) (Rad+(WxN-1)*pitchx)*sin(N*L) 0];
end;

At = [A(n,:); A]; % Vertice temp for easy calculation

for N = 2:1:(n+1),
    a(N-1,:) = At(N,:) - At(N-1,:); % a - vectors (in the direction of current flow)
end;

for Z = [1:1:Wy], % Calculate H at the Z-planes parallel to winding
    for X = [1:1:Xmax], % discrete x-steps for calculation purposes
        x = OuterRad/Xmax*X; % x of observer vector for X,Z iteration
        y = 0; % We assume rho symmetry
        z = 0.001+(Z-1)*pitchy; % z of observer vector; initial offset to
        % circumvent singularity
        R = [x y z]; % observer vector
        for N = 2:1:(n+1),
            b(N-1,:) = At(N-1,:) - R; % b-vector (to START of current stick)
            c(N-1,:) = At(N,:) - R; % c-vector (to END of current stick)
        end;
        for N = 1:1:n, % Calculate total H-field at observer R for each
            % stick n
            H = 1/(4*pi)*(cross(c(N,:),a(N,:))/(sum(cross(c(N,:),a(N,:)).^2))
                *(dot(a(N,:),c(N,:))/sqrt(sum(c(N,:).^2))dot(a(N,:),b(N,:))
                /sqrt(sum(b(N,:).^2))); % Biot-Savart stick model

            Hz(X,Z) = Hz(X,Z) + H(1,3); % filter z-component
        end;
        Xa(X) = x; % used for graphing purposes (if desired)
        Za(Z) = z; % ditto.
    end;
end;

Hzt = [Hz(:,1:(Wy-1)),Hz];
for coil = [2:1:Wy],
    Hzt(:,coil-1) = Hz(:,Wy-coil+2); % generate matrix of hieght 2*Wn to calculate H
end;

for coil = 1:1:Wy, % which coil are we currently calculating M
    for X = 1:1:Wx, % for which X-layer is coupling calculated
        for Y = 1:1:Wy, % for which Y-layer we calculate coupling
            clear flux; % initialise flux vector
            for r = 1:1:(ceil((Rad+(X-1)*pitchx)/OuterRad*Xmax)),
                % width of target loop (radius)
                AnulusArea = (r^2 - (r-1)*(r-1))*(OuterRad/Xmax)^2*pi;
                % calculate area of each annulus
                flux(r) = uo*AnulusArea*Hzt(r,(Y-coil+Wy));
                % Simpsons rule
            end;
        end;
    end;
end;

```

```
fluxXY(Wy*(X-1)+Y,coil)=sum(flux,2);  
                                % flux linkages of coil for all coils in inductor  
end;  
end;  
end;
```

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